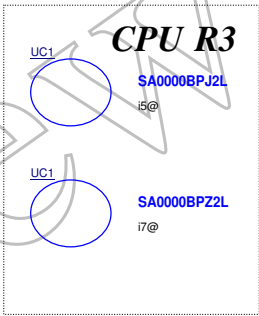
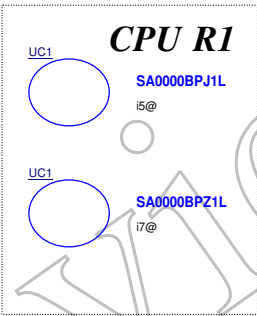
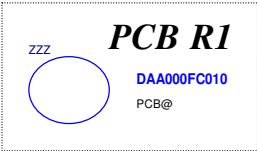


COMPAL CONFIDENTIAL

MODEL NAME : Loki-G 15/17
MB PCB PN : DAA000FC010
PWR/B PCB PN : DA4002L3010
IO/B PCB PN : DA6001XF010



Dell/Compal Confidential

Schematic Document

COFFEE LAKE H


N17P-G0/G1

Loki-G 15/17

2018-03-22

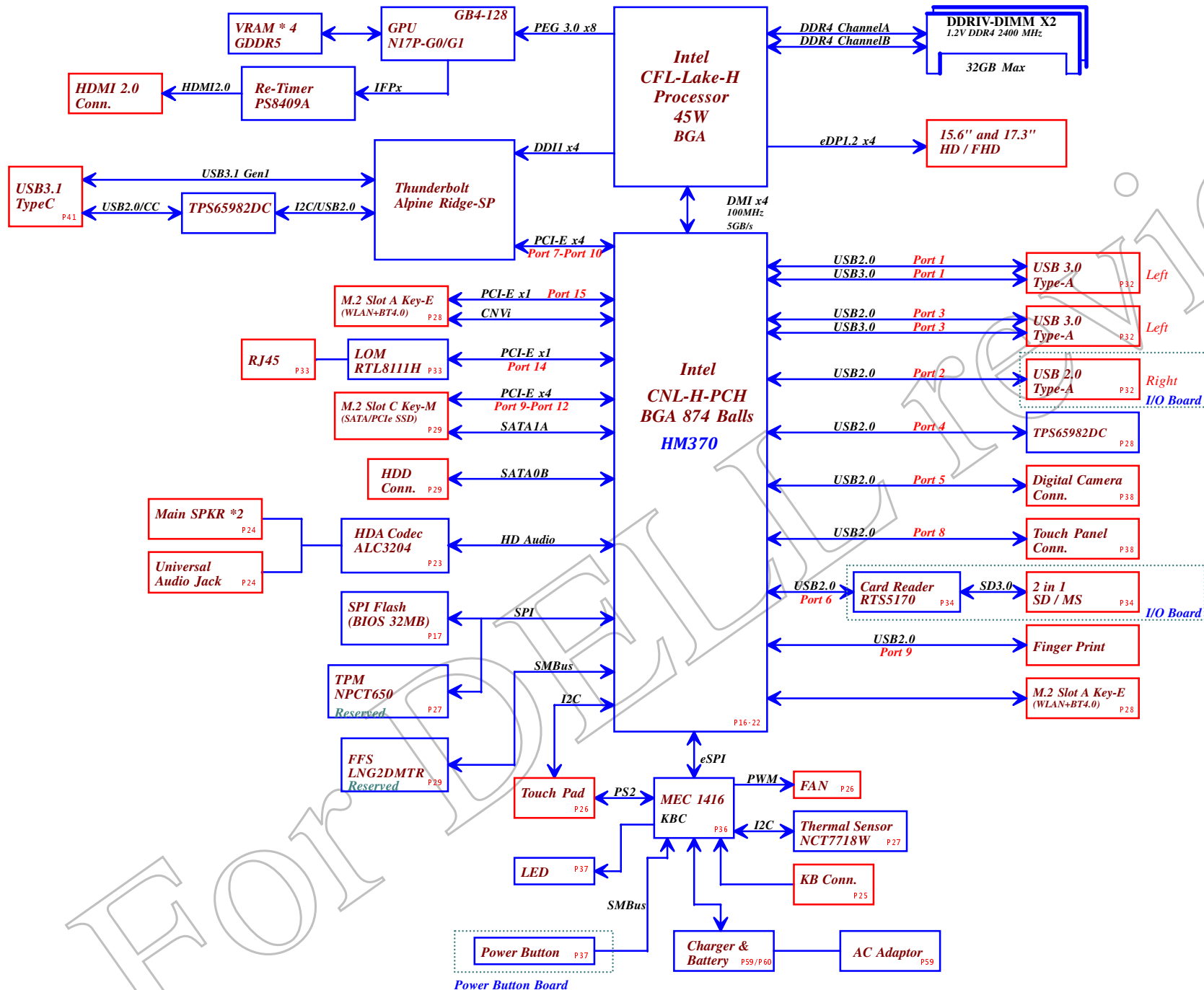
REV : 1.0 (A00)

Layout Dell logo



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REV: X00
PWB: 9HTP8

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128M*32 x4 =2G
256M*32 x4 =4G

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Board ID	Resistor
X00	100K
X01	17.8K
X02	27K
X03	37.4K
A00	49.9K

HSIO port Allocation

USB3	DESTINATION
1	USB JUSB1 (Left Side)
2	None
3	USB JUSB3 (Left Side)
4	None
5	None
6	None

USB2	DESTINATION
1	USB JUSB1 (Left Side)
2	USB JUSB2 (I/O)
3	USB JUSB3 (Left Side)
4	TYPE-C PD
5	CAMERA
6	Card Reader (I/O)
7	BT & CNVi BRI
8	Touch Screen
9	Finger Print
10	None
11	None
12	None
13	None
14	None

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	None	7	None
Lane 2	None	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	NGFF - NVMe SSD		
Lane 10		SATA	DESTINATION
Lane 11		0a	None (NVMe)
Lane 12		1a	NGFF - SSD
Lane 13		None (HDD)	0b
Lane 14	LAN	1b	None (LAM)
Lane 15	NGFF - WLAN	2	None (WLAN)
Lane 16	None	3	None
Lane 17	None	4	None
Lane 18	None	5	None
Lane 19	None	6	None
Lane 20	None	7	None
Lane 21	Alpine Ridge - SP		
Lane 22			
Lane 23			
Lane 24			

Table 1-7. PCH HSIO Detail (SKU 9-11 of 11)

Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI2.0 LSPCON PS175

eSPI Virtual Wires (VW) (Sheet 1 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SUS_STAT#	Output	ESPI_RESET#	No
SUS_PWRDN_ACK	Output	ESPI_RESET#	No
PLTRST#	Output	ESPI_RESET#	Yes
PME#	Input	ESPI_RESET#	No
WAKE#	Input	ESPI_RESET#	No
SMI#	Input	PLTRST#	N/A
SCI#	Input	PLTRST#	N/A
RCIN#	Input	PLTRST#	No
SLP_A#	Output	ESPI_RESET#	Yes

eSPI Virtual Wires (VW) (Sheet 2 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SLP_S3#/SLP_S4#/ SLP_SS#/SLP_LAN#/ SLP_WLAN#	Output	DSW_PWROK	Yes



CLK_PCIE	DESTINATION	CLK_REQ	DESTINATION
0	TBT-AR	0	TBT-AR
1	None	1	None
2	None	2	None
3	None	3	None
4	None	4	None
5	None	5	None
6	None	6	None
7	GPU	7	GPU
8	None	8	None
9	NGFF - SSD	9	NVMe
10	None	10	None
11	None	11	None
12	None	12	None
13	None	13	None
14	LAN	14	LAN
15	WLAN	15	WLAN

13.2.1 Coffee Lake PCH-H

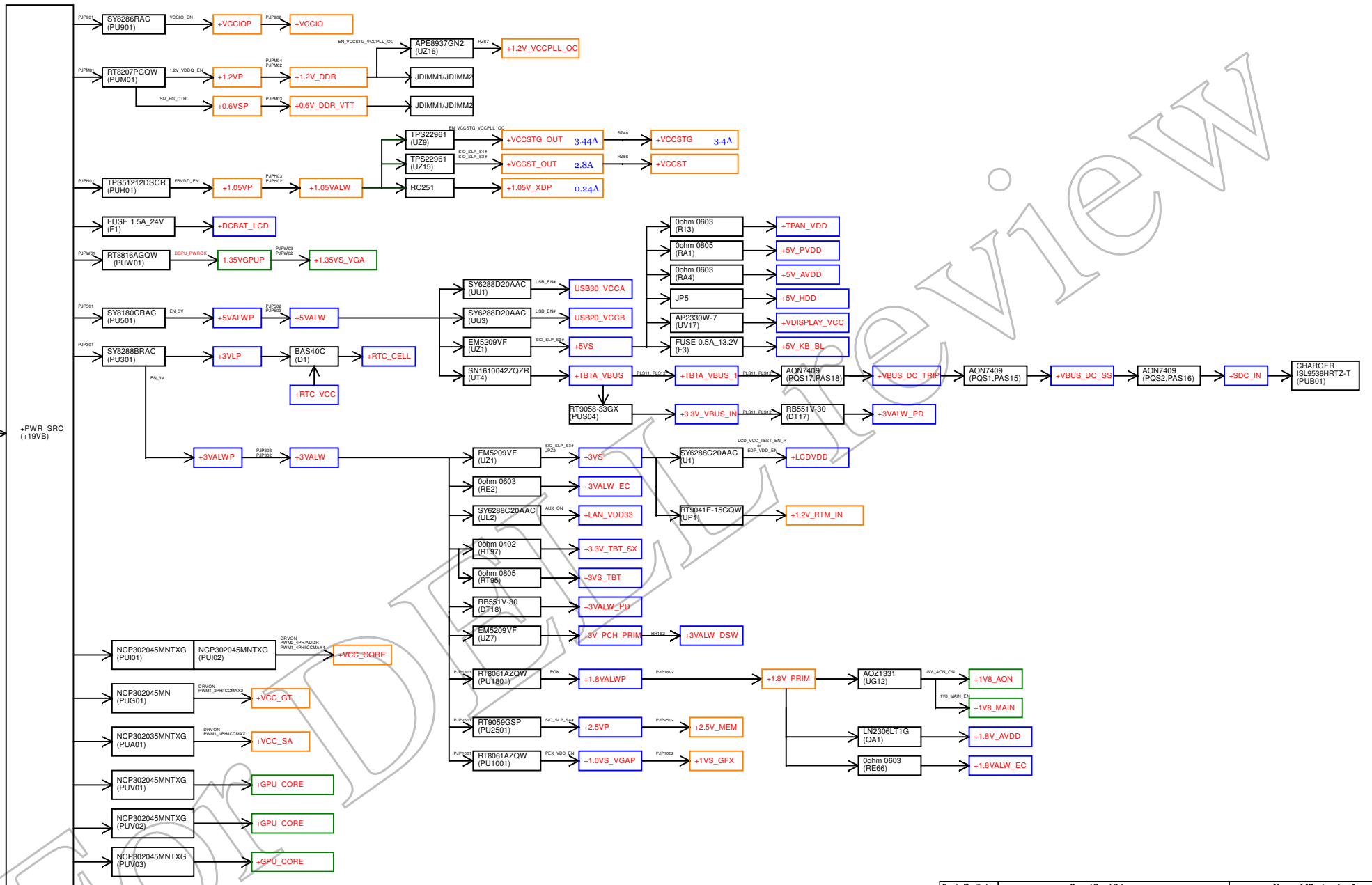
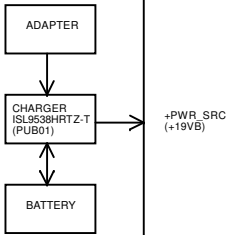
Figure 13-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

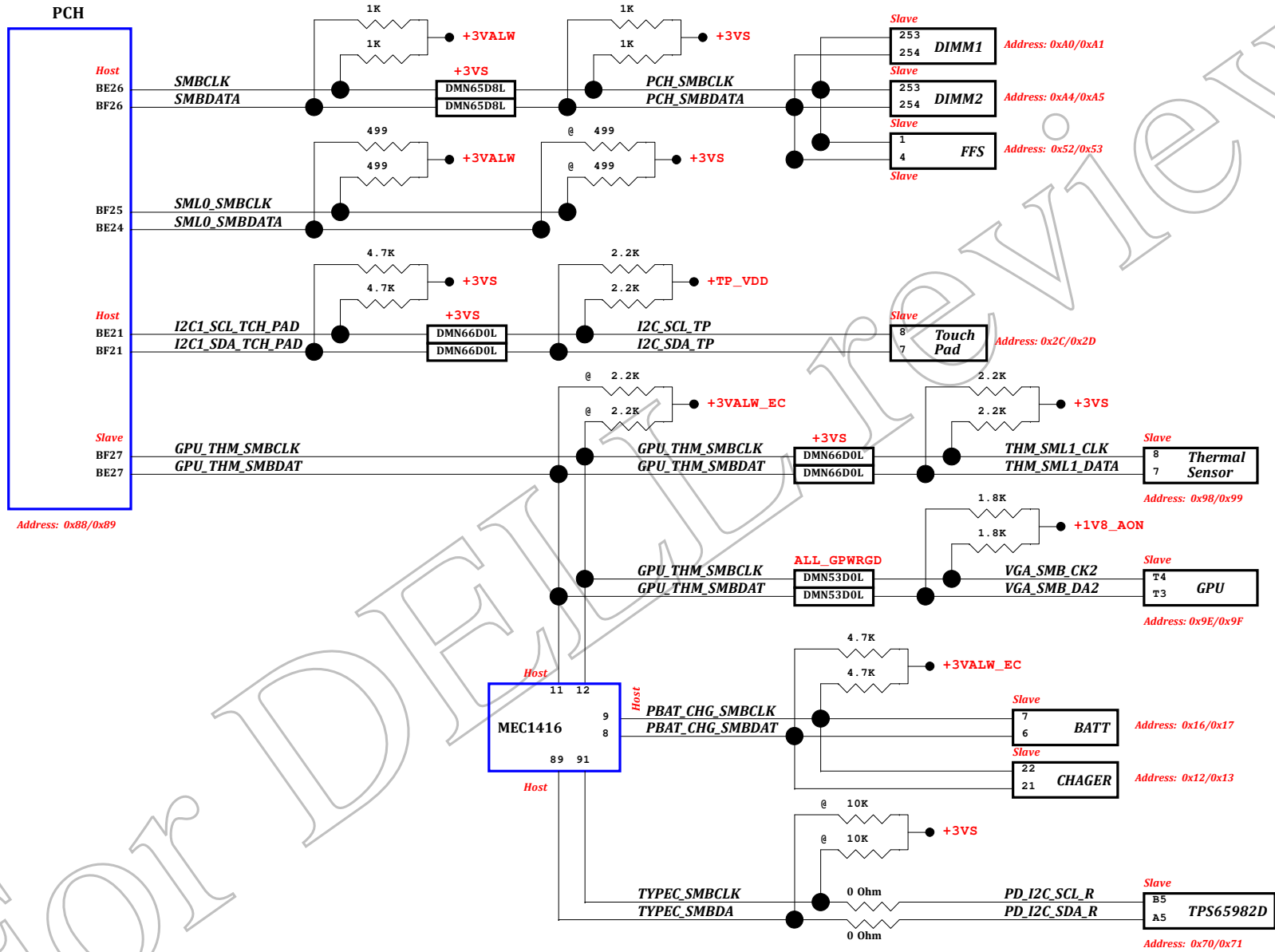
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29			
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	PCIe* #2	USB3.1 #8	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	SATA 1a	SATA 1b	SATA 1c	SATA 2	SATA 3	SATA 4	SATA 5	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support									No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support

Symbol Note :

 : means Digital Ground
 : means Analog Ground

CPU PWR
GPU PWR
Peripheral Device PWR





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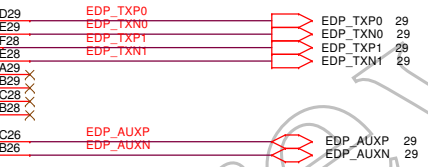
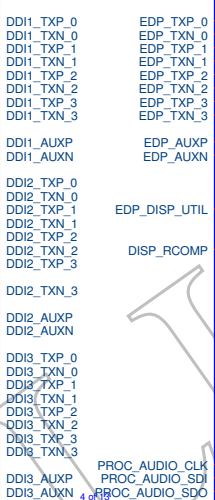
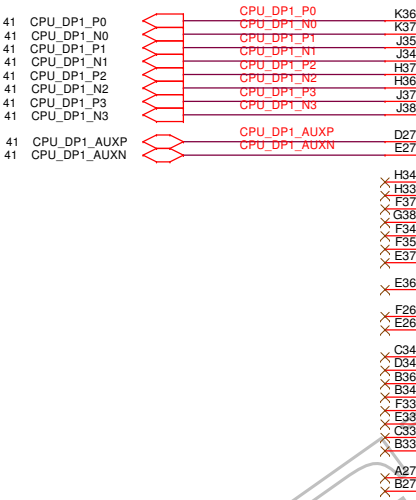
Main Func = CPU

TBT-AR

UC1
CFL_H@
CFL-H_BGA1440
SA011703151

CFL_H_SOC

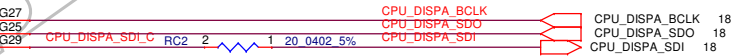
UC1D



eDP



DP_RCOMP
Trace width=5 mils
Spacing=20 mils
Max length= 600 mils

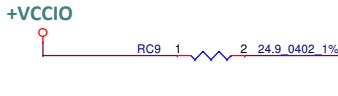
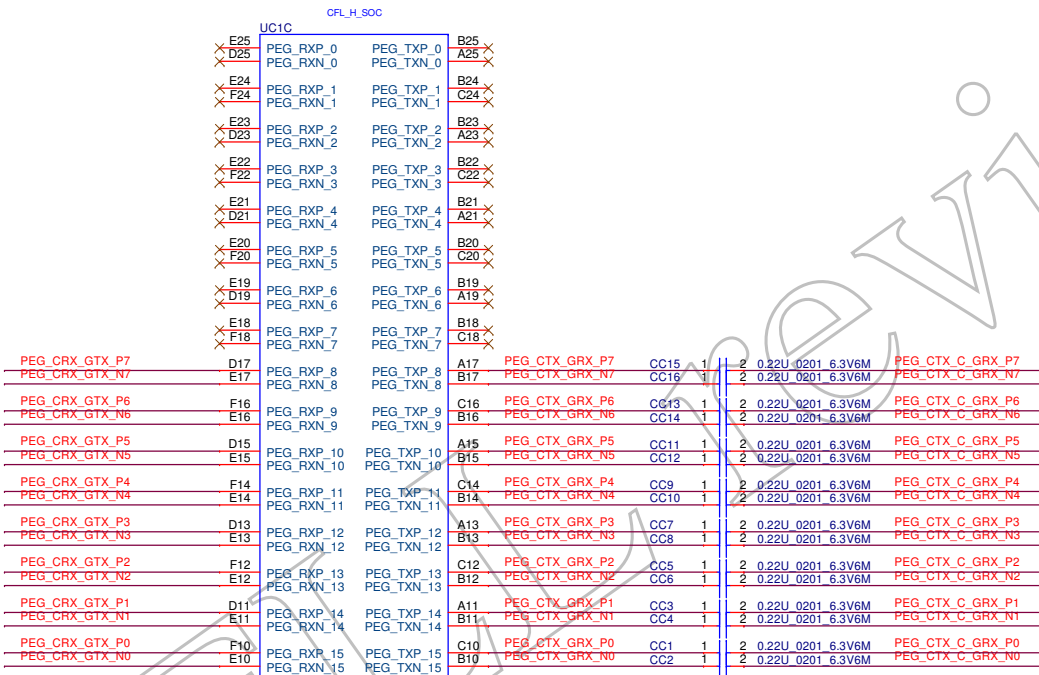
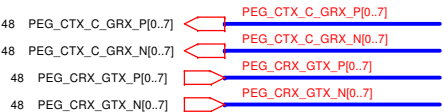


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								Size		Document Number		Rev	
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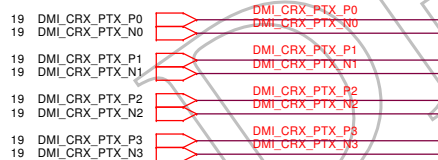

```
15  DDR_B_D[0..63]
```



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From PCH



To PCH

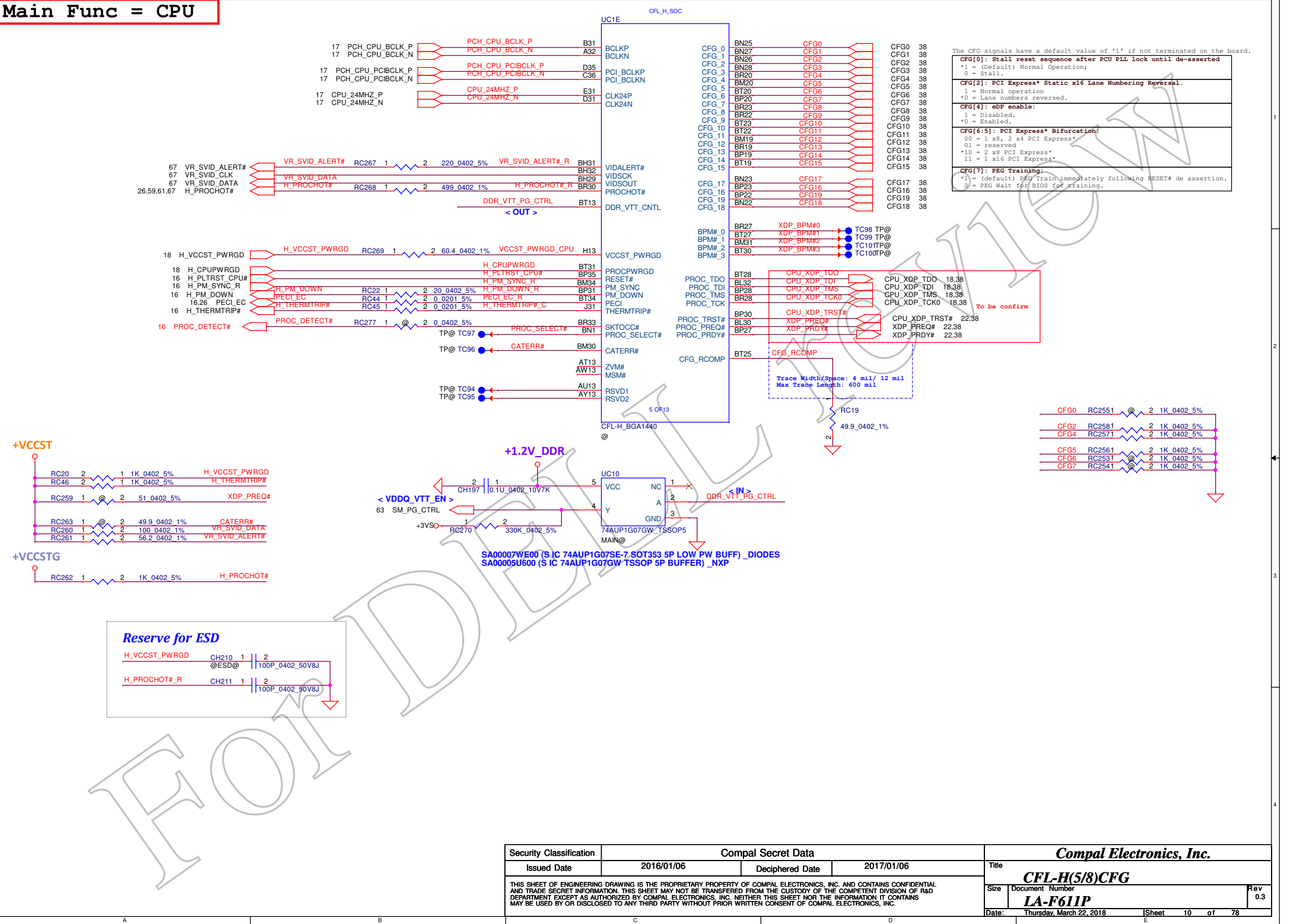
PEG_RCOMP

Trace width=15 mils

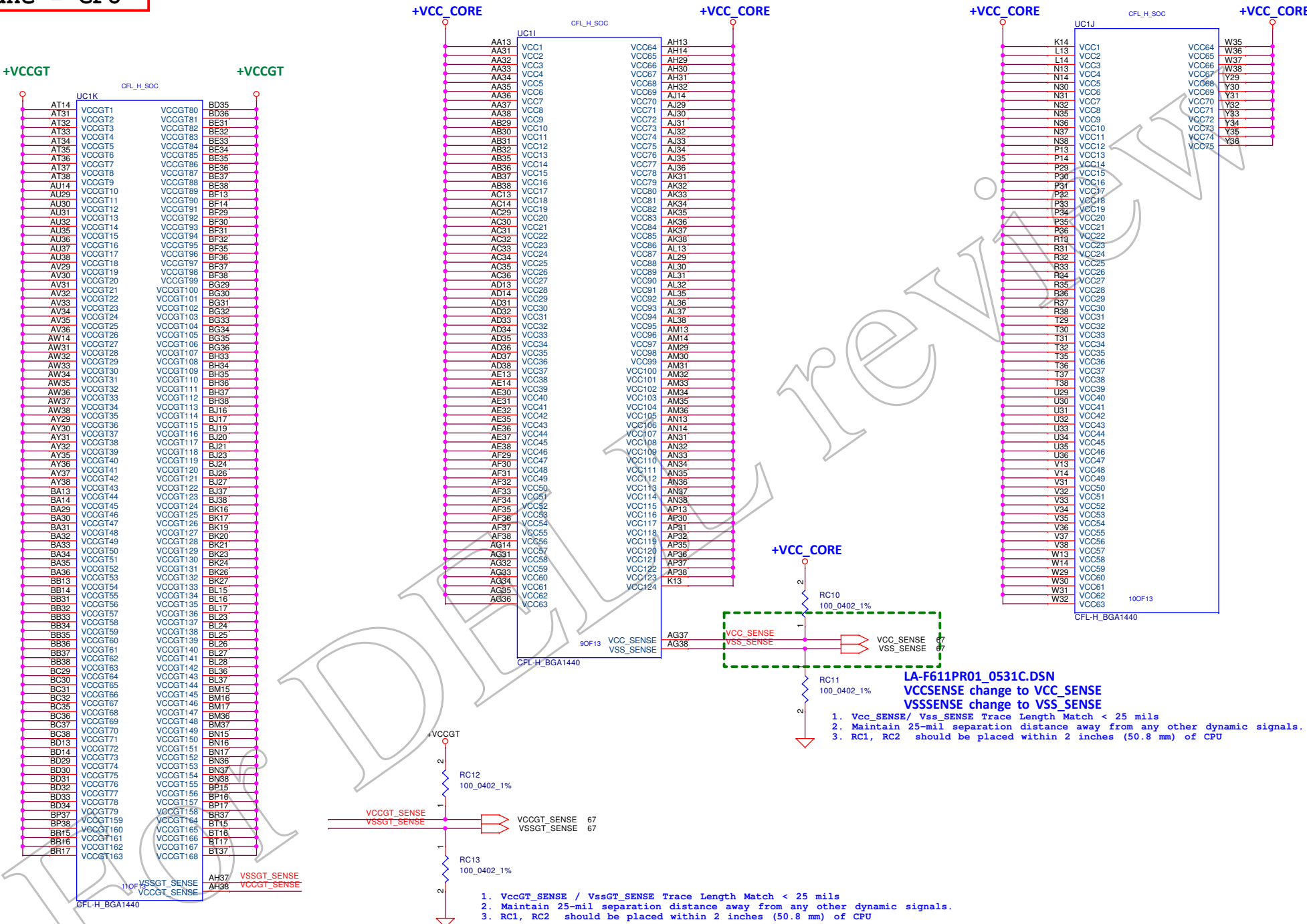
Spacing=15 mils

Max-length= 600 mils

Main Func = CPU

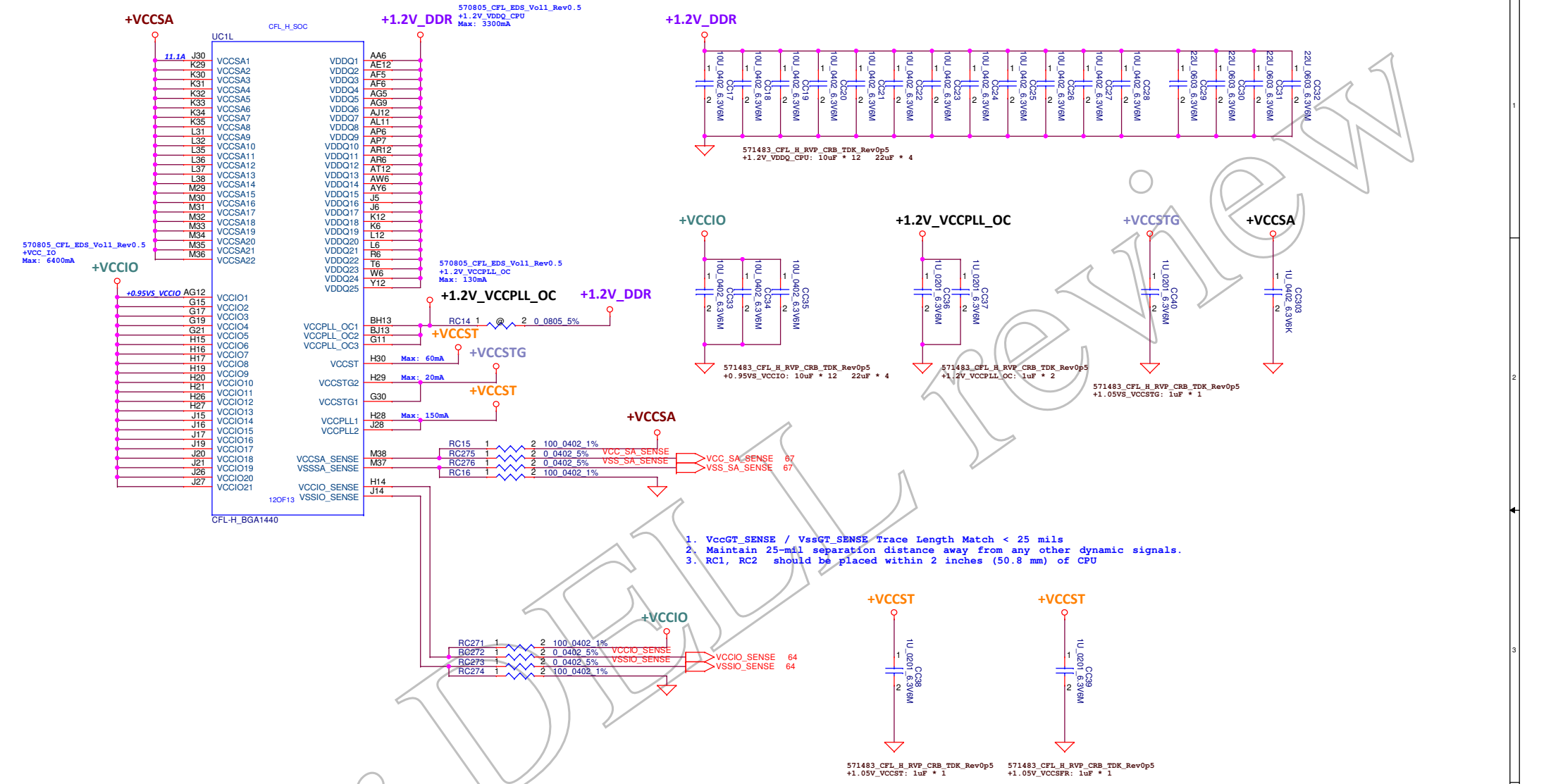


Main Func = CPU



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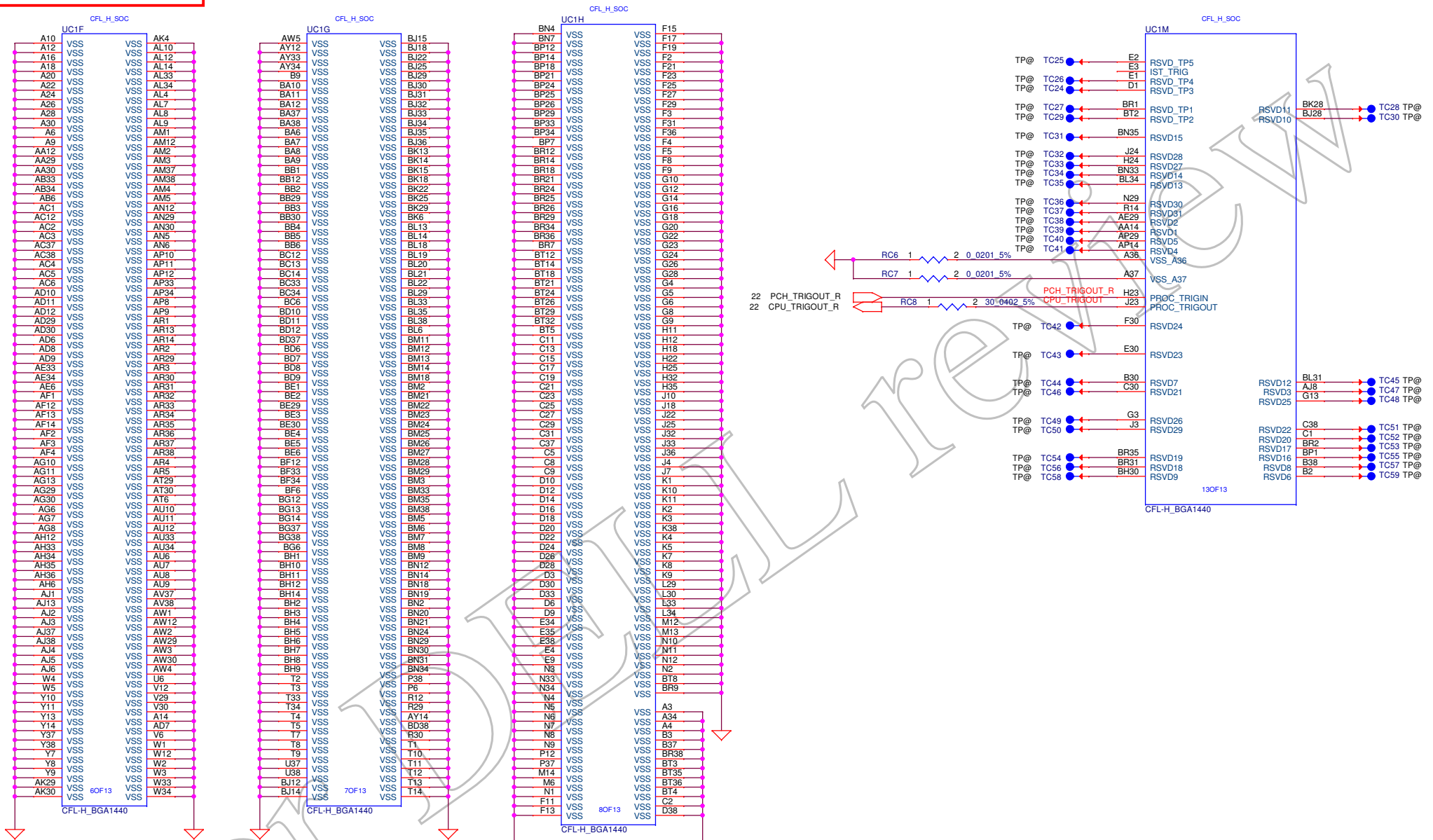
Main Func = CPU



- 1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
- 2. Maintain 25-mil separation distance away from any other dynamic signals.
- 3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

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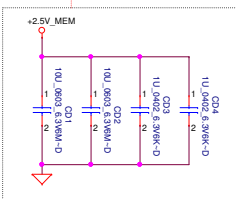
Main Func = CPU



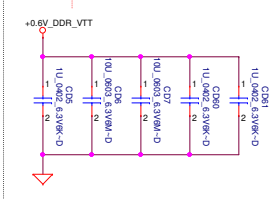
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Main Func = DDR

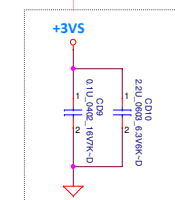
Layout Note:
Place near JDIMM1.257,259



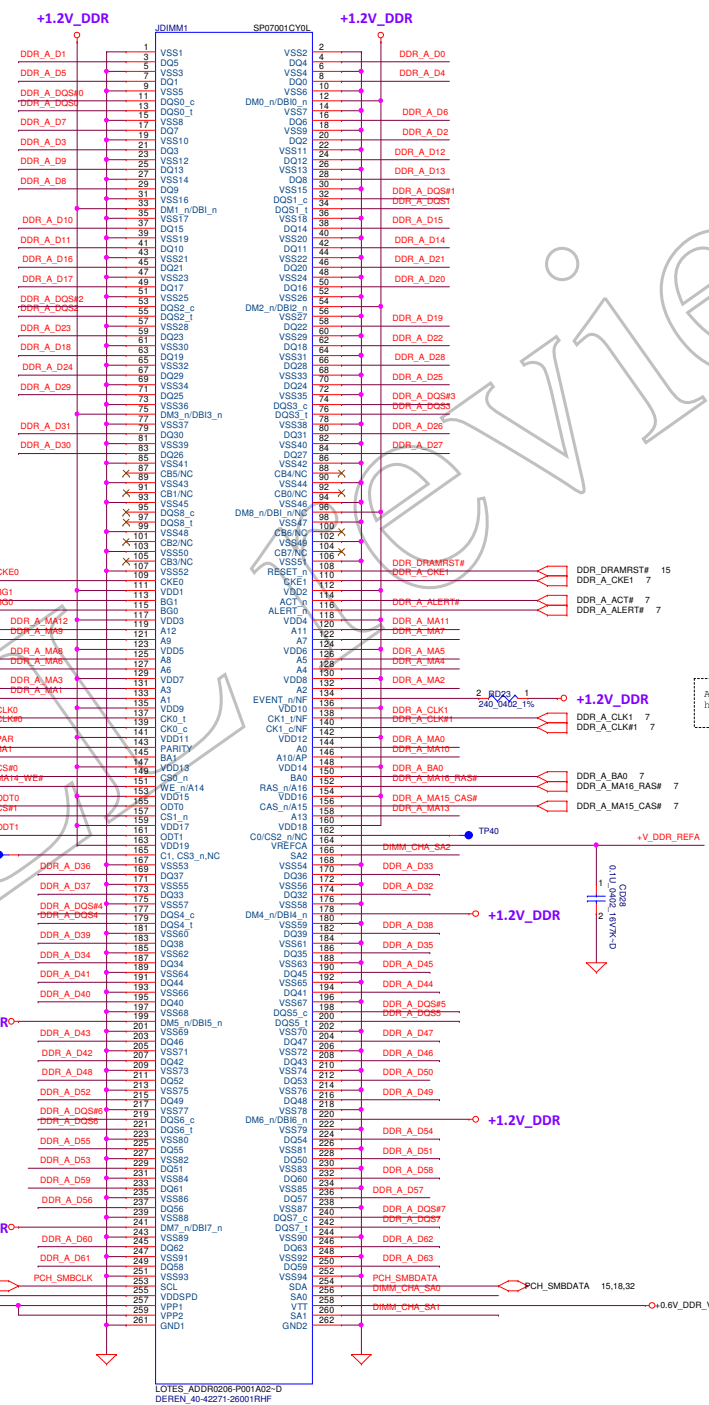
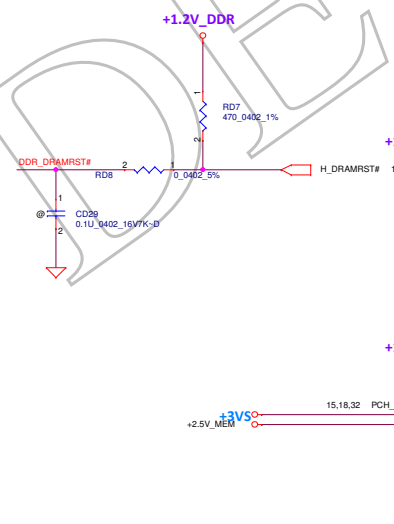
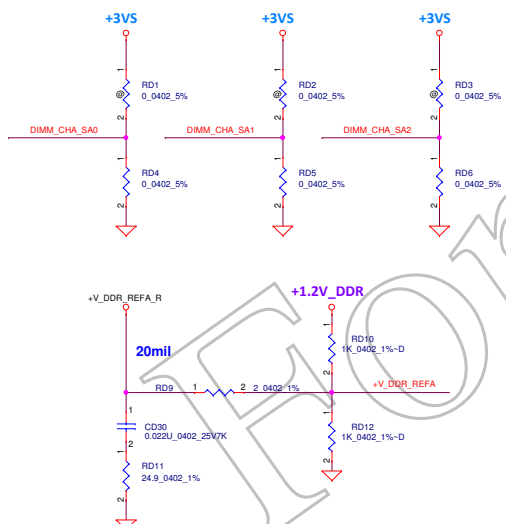
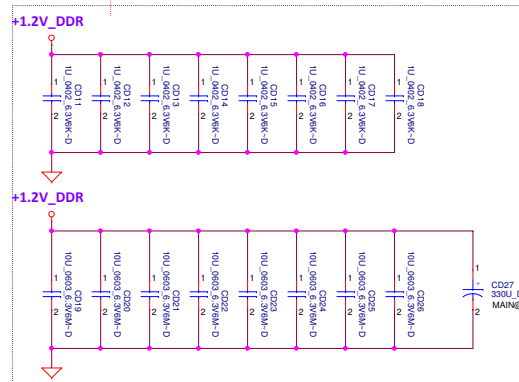
Layout Note:
Place near JDIMM1.258



Layout Note:
Place near JDIMM1.255



Layout Note:
Place near JDIMM1

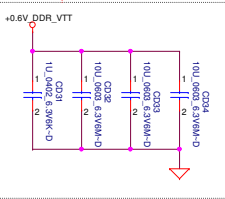


All VREF traces should have 10 mil trace width

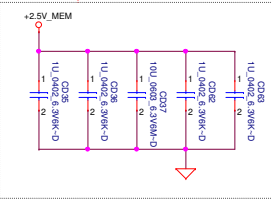
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Main Func = DDR

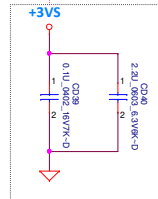
Layout Note:
Place near JDIMM2.258



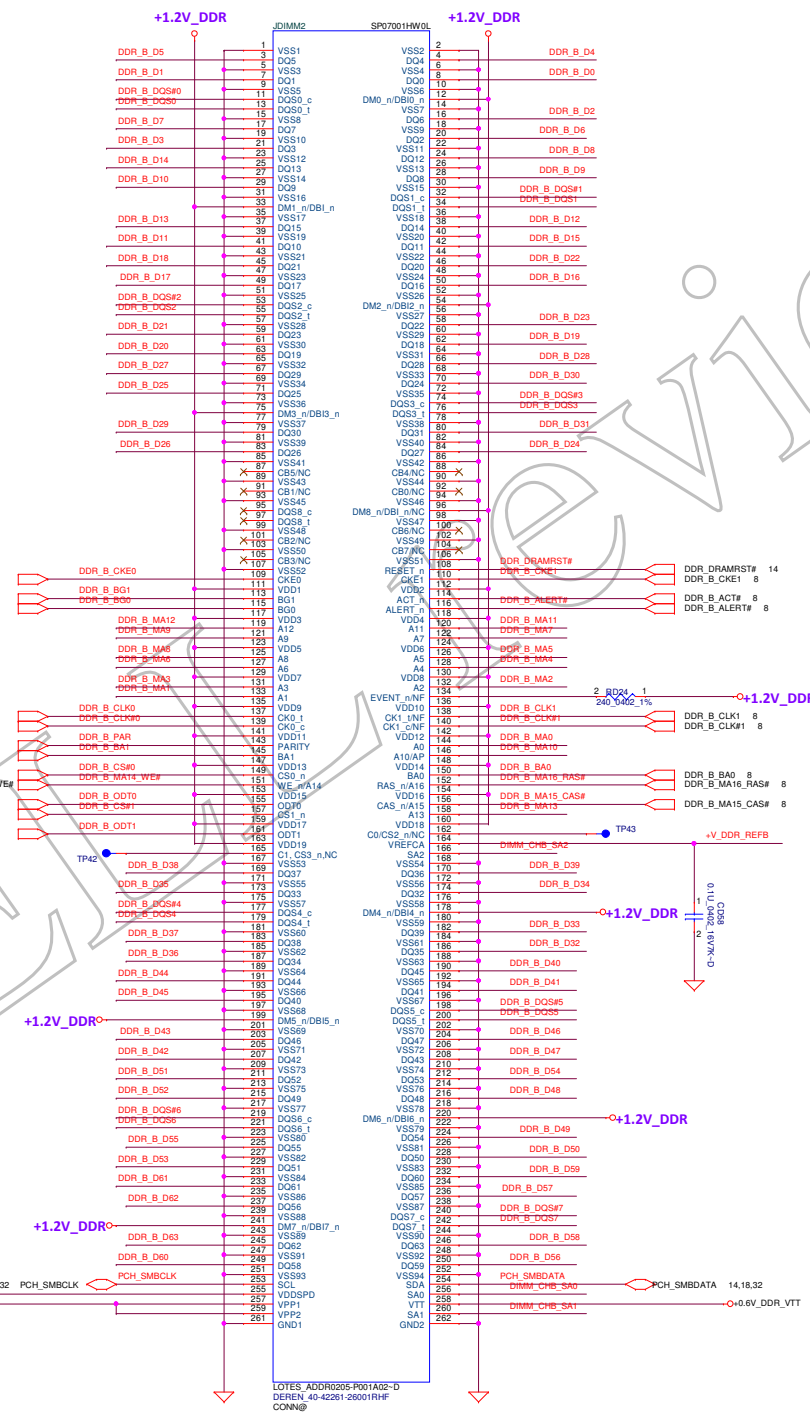
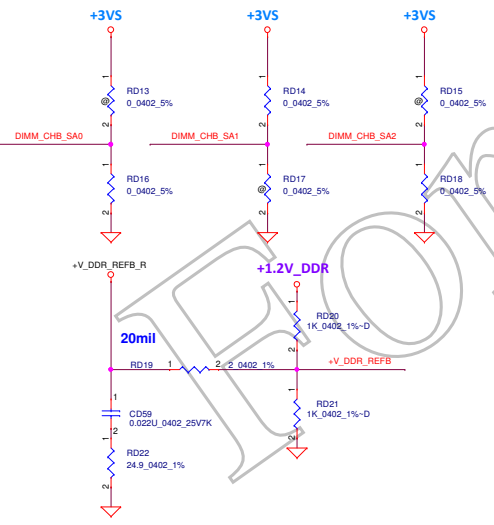
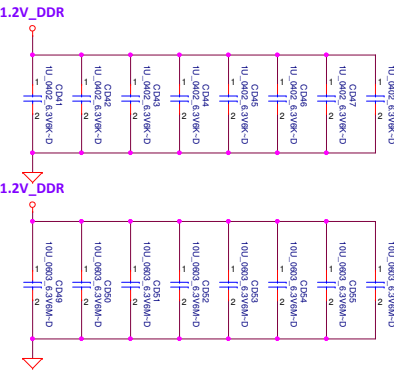
Layout Note:
Place near JDIMM2.257,259



Layout Note:
Place near JDIMM2.255



Layout Note:
Place near JDIMM2



All VREF traces should
have 10 mil trace width

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				0.3	
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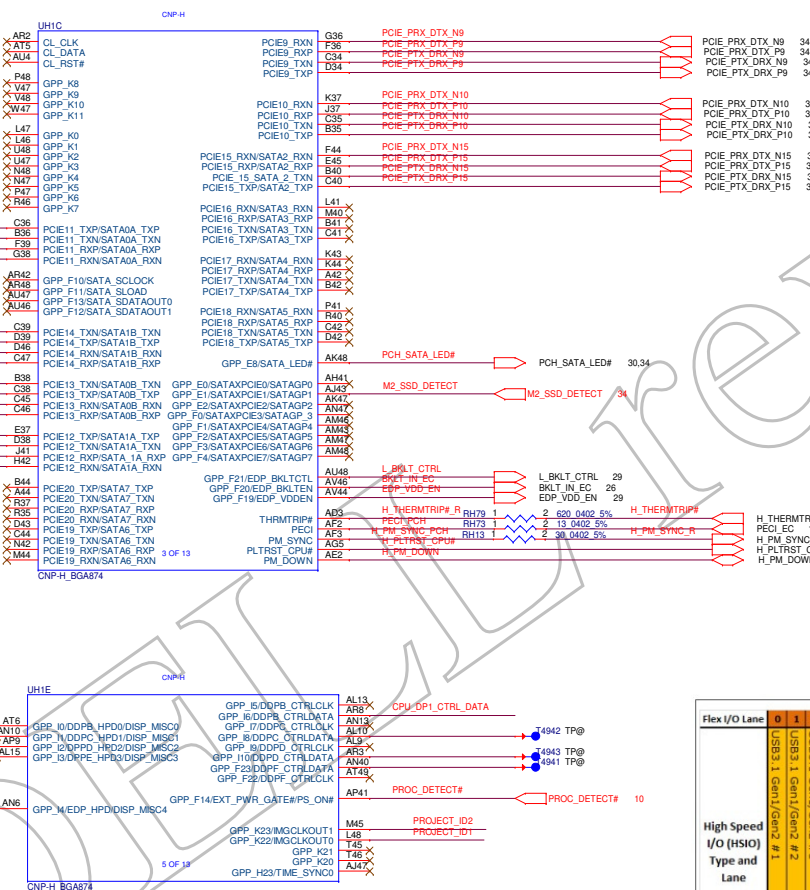
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ¹	None ²	None ³

34	PCIE_PTX_DRX_P11	PCIE_PTX_DRX_P11
34	PCIE_PTX_DRX_N11	PCIE_PTX_DRX_N11
34	PCIE_PRX_DTX_P11	PCIE_PRX_DTX_P11
34	PCIE_PRX_DTX_N11	PCIE_PRX_DTX_N11

35	PCIE_PTX_DRX_N14	PCIE_PTX_DRX_N14
35	PCIE_PTX_DRX_P14	PCIE_PTX_DRX_P14
35	PCIE_PRX_DTX_N14	PCIE_PRX_DTX_N14
35	PCIE_PRX_DTX_P14	PCIE_PRX_DTX_P14

32	SATA3_PTX_DRX_N0	SATA3_PTX_DRX_P0	SATA3_PTX_DRX_N0
32	SATA3_PTX_DRX_P0	SATA3_PTX_DRX_N0	SATA3_PTX_DRX_P0
32	SATA3_PRX_DTX_N0	SATA3_PRX_DTX_P0	SATA3_PRX_DTX_N0
32	SATA3_PRX_DTX_P0	SATA3_PRX_DTX_N0	SATA3_PRX_DTX_P0

34	PCIE_PTX_DRX_P12	PCIE_PTX_DRX_P12
34	PCIE_PTX_DRX_N12	PCIE_PTX_DRX_N12
34	PCIE_PRX_DTX_P12	PCIE_PRX_DTX_P12
34	PCIE_PRX_DTX_N12	PCIE_PRX_DTX_N12



PROJECT ID	PROJECT ID1 (GPP_K22)
Non-TBT	0
TBT	1

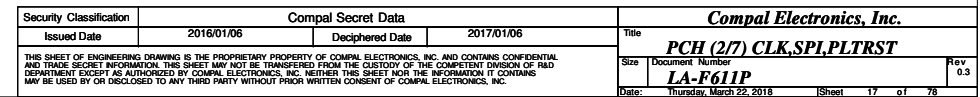
TPM ID	PROJECT ID2 (GPP_K23)
SW TPM	0
HW TPM	1

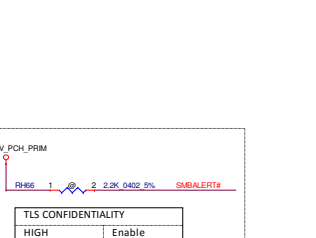
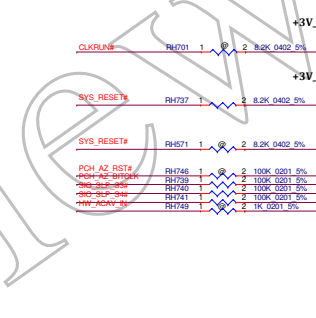
CPU_DPI_CTRL_DATA RH33 1 2.2K 0402 2 5%

[illegible]

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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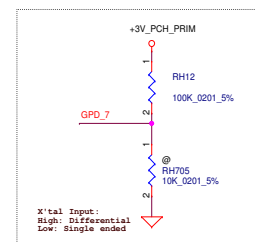


V_PCH_PRIM

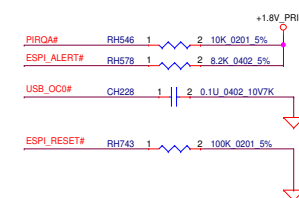
R#64 2 2.2K 0.402 5% SMU_ALERT#

EC interface	
HIGH	ESPI*
LOW(DEFAULT)	LPC

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USB3.0 Port1



USB3.0 Port2

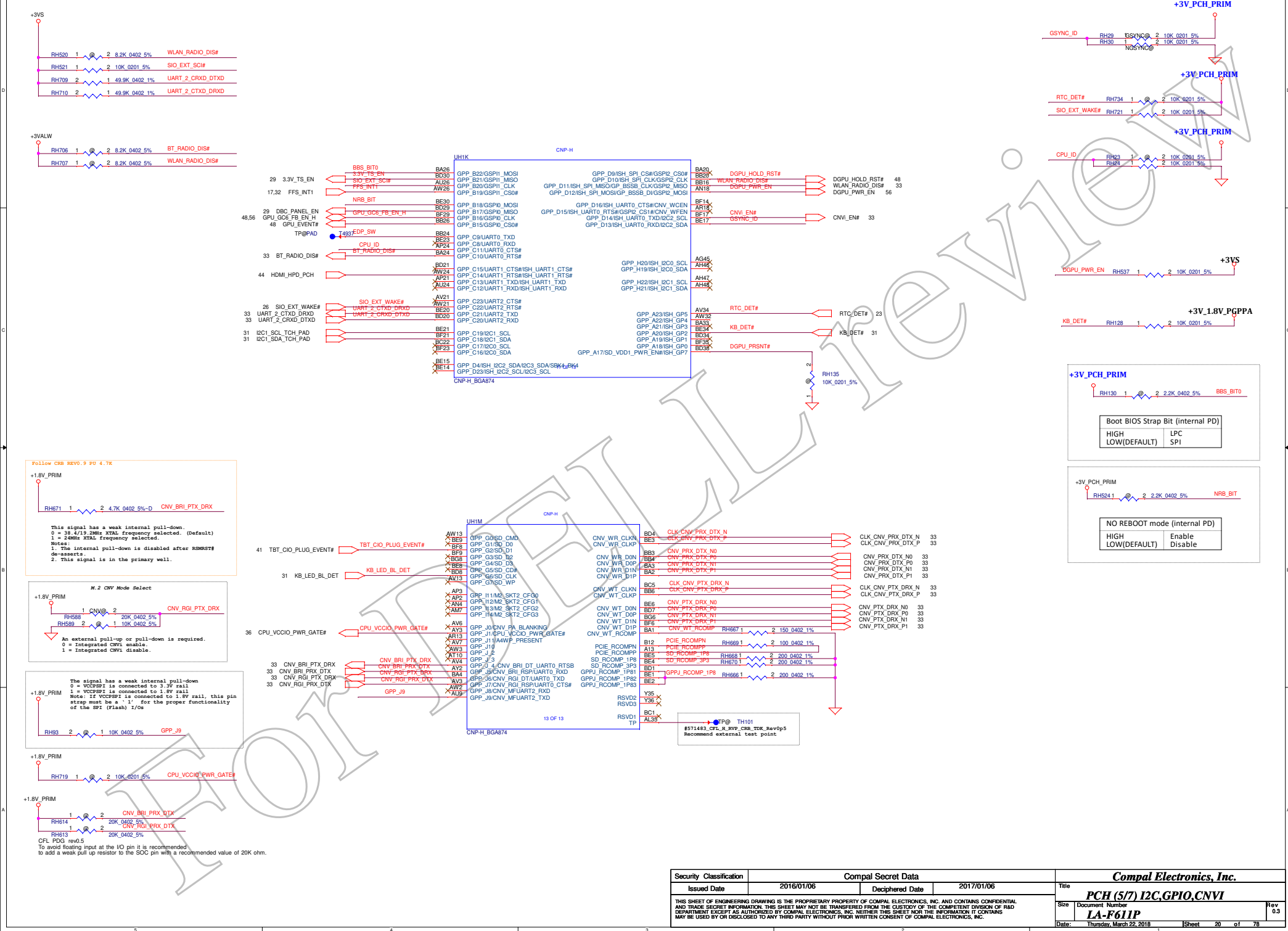
Reserve for EMI

ESPI_CLK CC57 2 | 1 12P_0402_50V8J

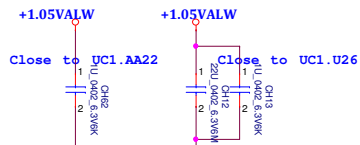
@EMI@

Security Classification		Compal Secret Data		Compal Electronics, Inc.						
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						PCH (4/7) DMLPCIE,USB,LPC				
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						Document Number				
						LA-F61IP				
Date: Thursday, March 22, 2018										
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Main Func = PCH

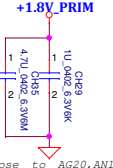
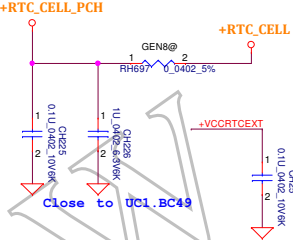
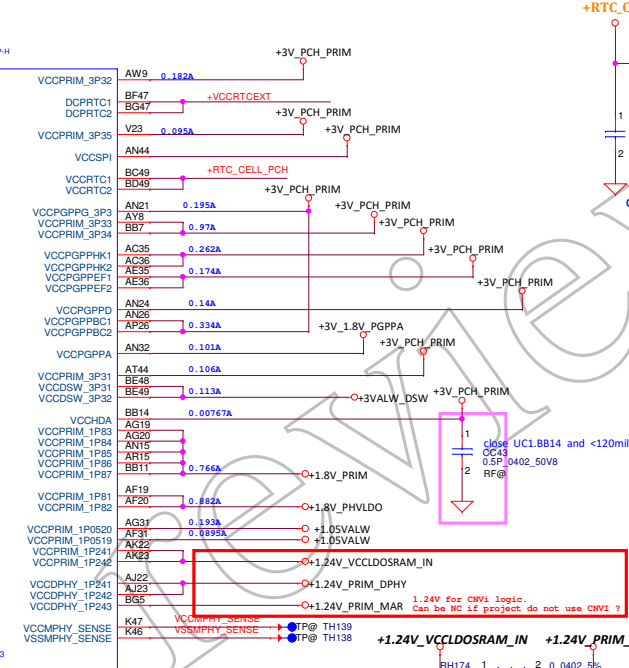
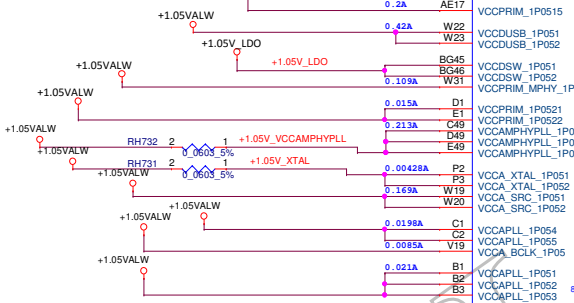
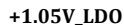


Main Func = PCH

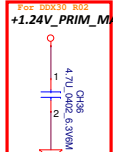


PLACE 3-5MM FROM PACKAGE EDGE

Deep Sx Well: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.



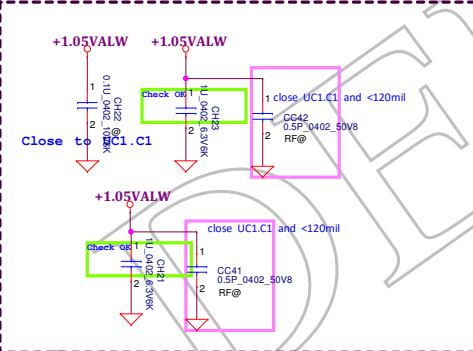
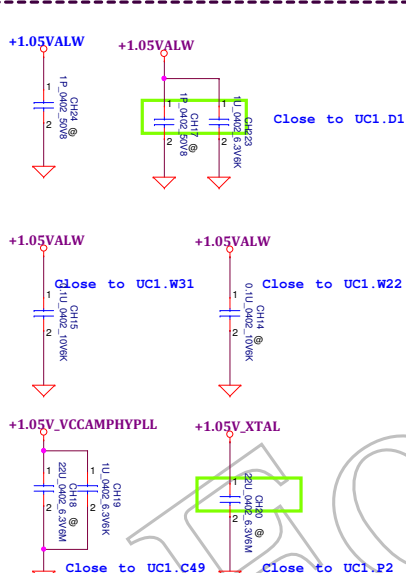
Close to AG20, AN15



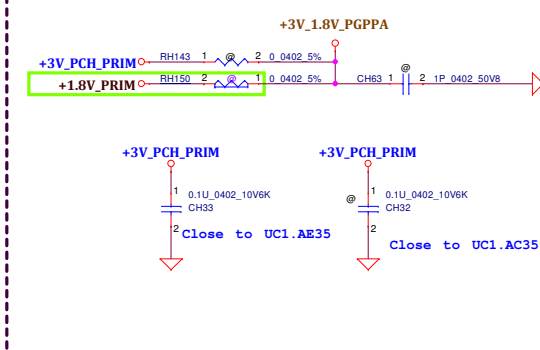
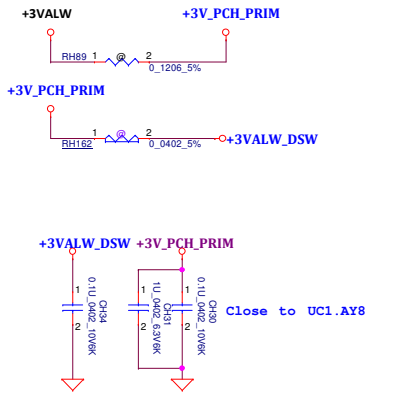
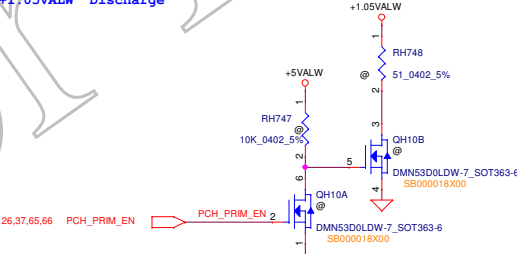
For DDX30 R02

+1.24V VCCLDOSRAM IN +1.24V PRIM DPHY

RH174 for 571391 CFL H PDG Rev0p71.ppt



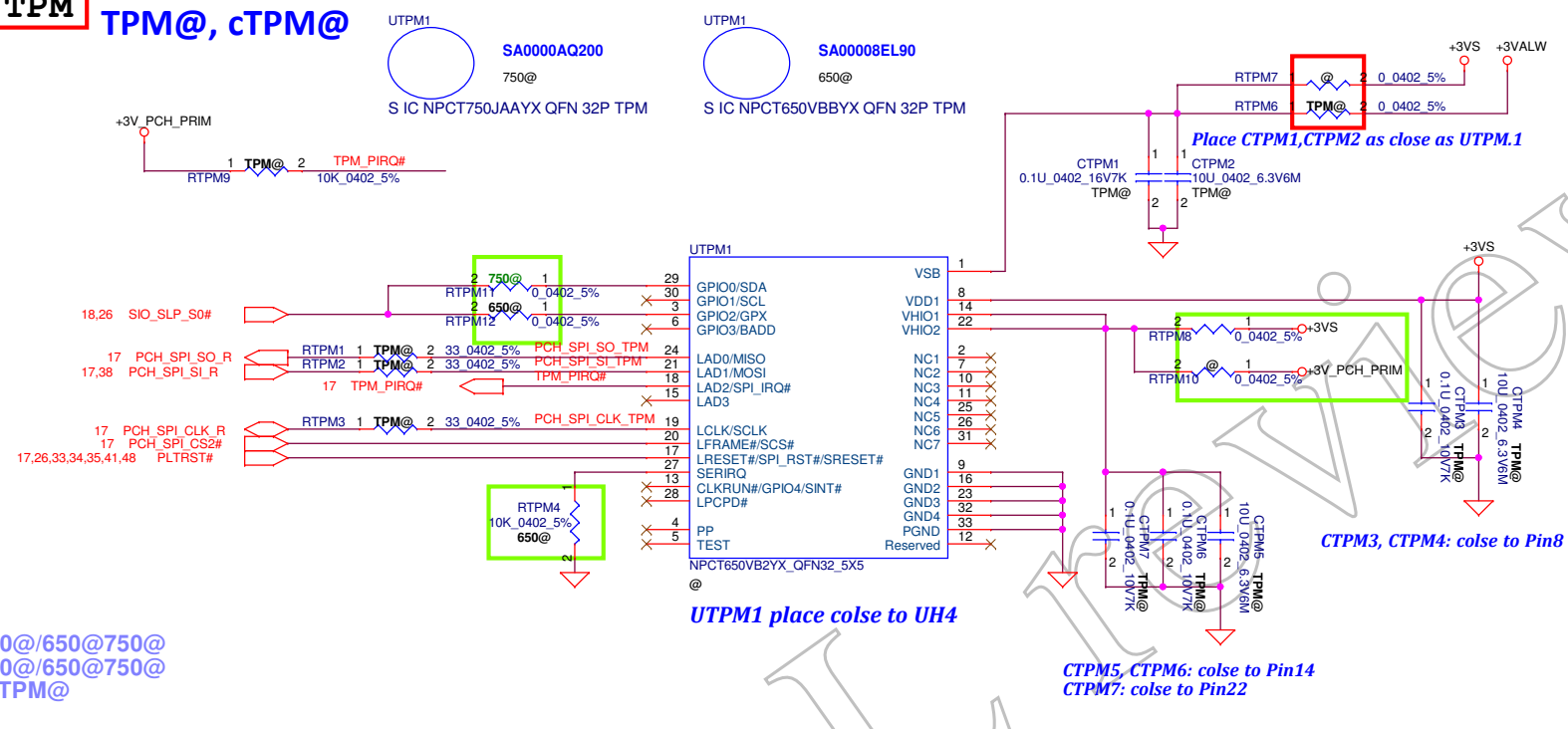
+1.05VALW Discharge



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Main Func = TPM

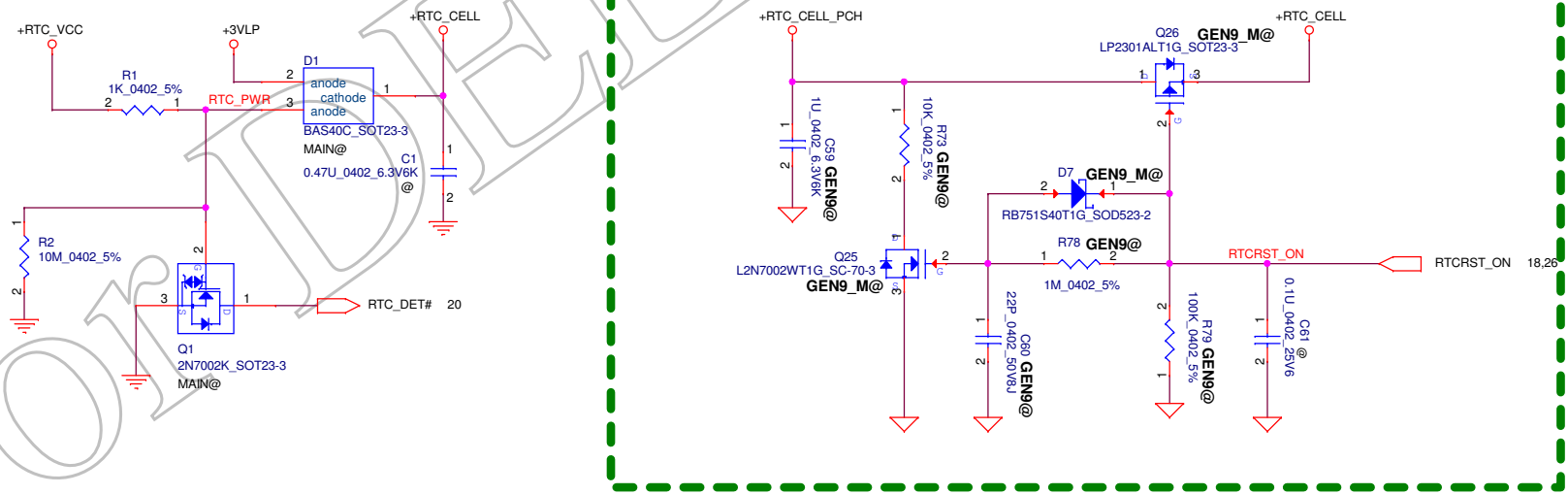
TPM@, cTPM@



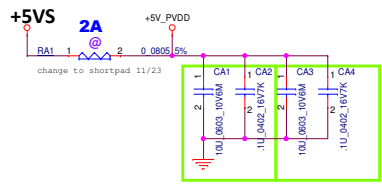
NPCT650:TPM@/650@/650@750@
NPCT750:TPM@/750@/650@750@
ChinaTPM:TPM@/cTPM@
SW TPM:tTPM@

Main Func = RTC

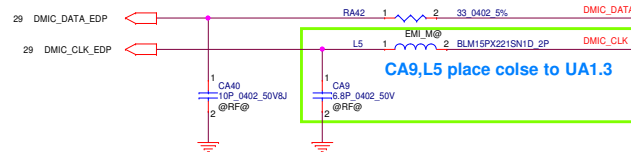
GEN9@



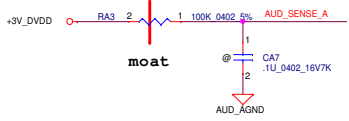
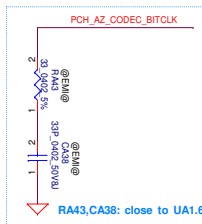
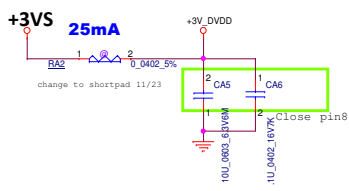
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2016/01/06		Deciphered Date		2017/01/06		Title			
								TPM/RTC/Screw Holes			
								Size		Document Number	
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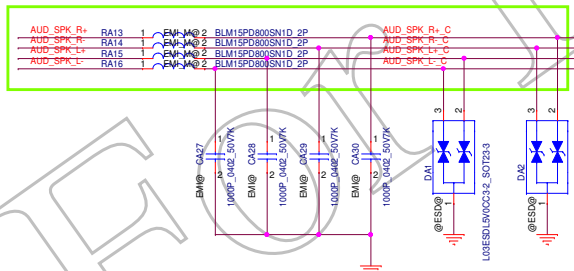
Layout Note: Close pin39
Layout Note: Close pin34



CA9,L5 place close to UA1.3

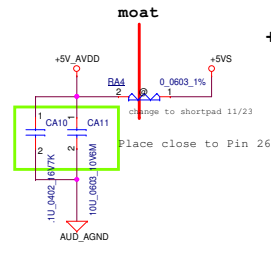
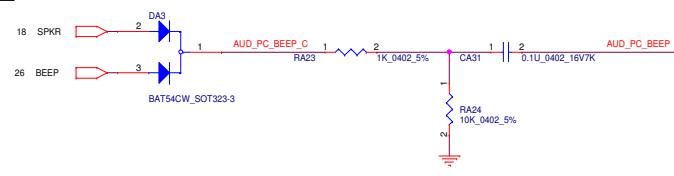


Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

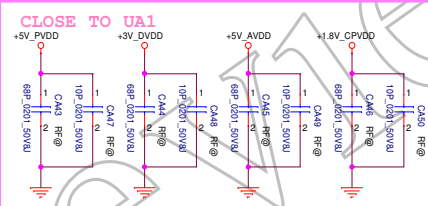


Speaker

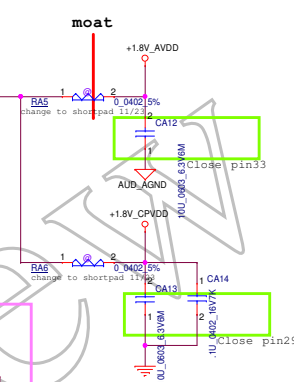
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



+1.8V_PRIM



CLOSE TO UA1



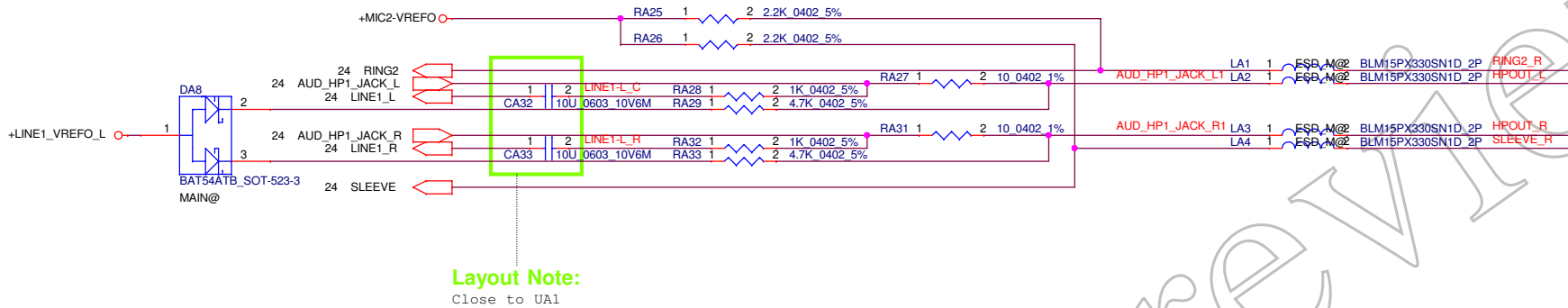
Layout Note: Tied at point only under Codec or near the Codec

Place on the moat between GND & GNDA.

Main Func = Audio Jack

ESD@

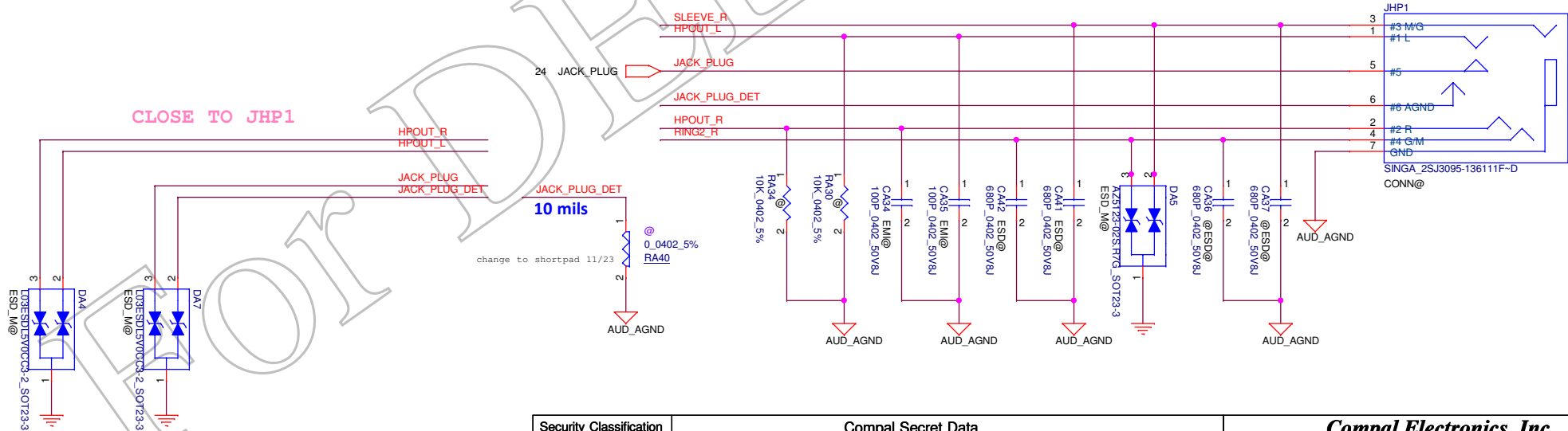
Universal Jack
(Global Headset Jack + mic phone in + line in support)



Main Func = Audio Jack

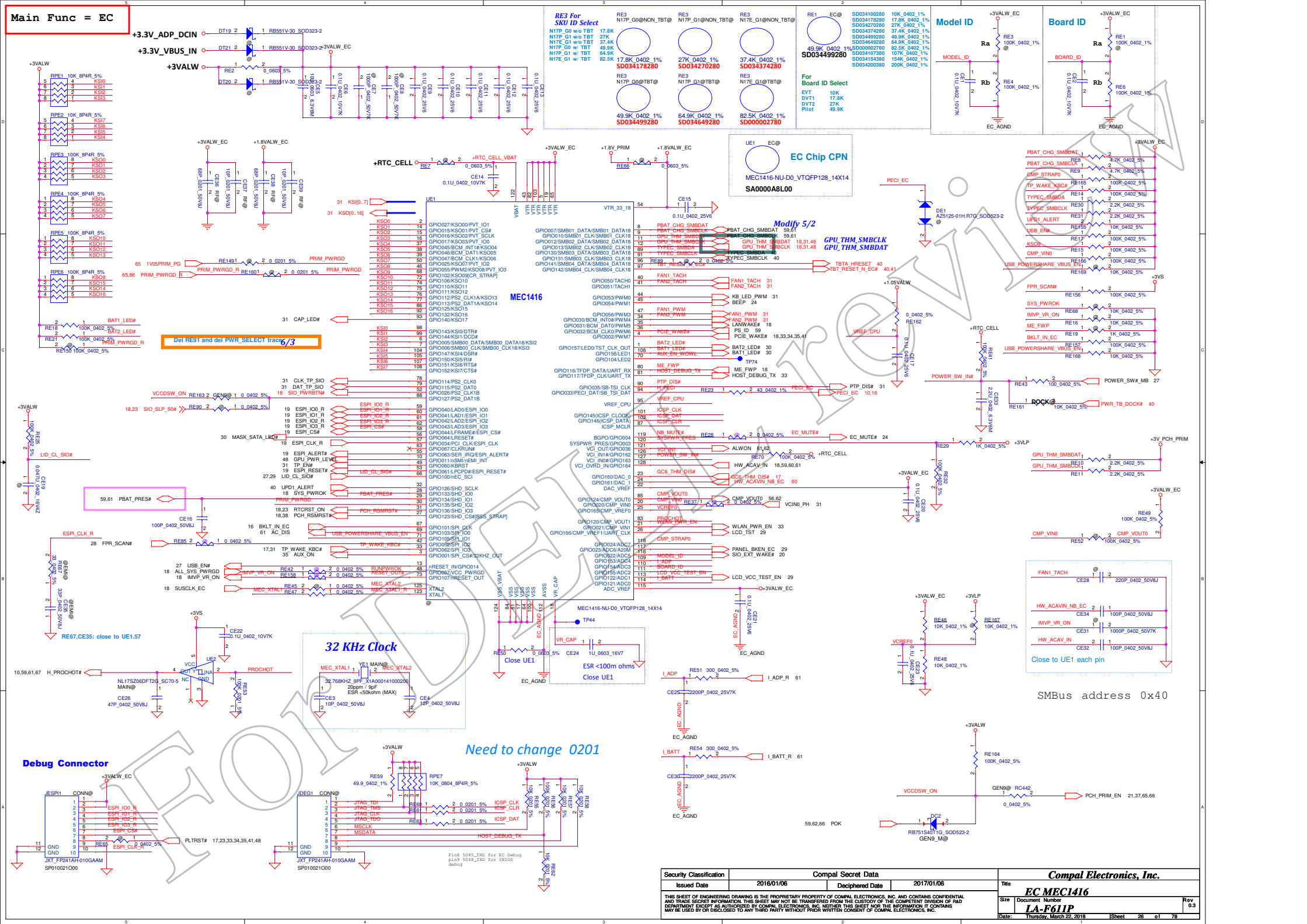
EMI@, @ESD@, ESD@

Universal Jack
(Global Headset Jack + mic phone in + line in support)

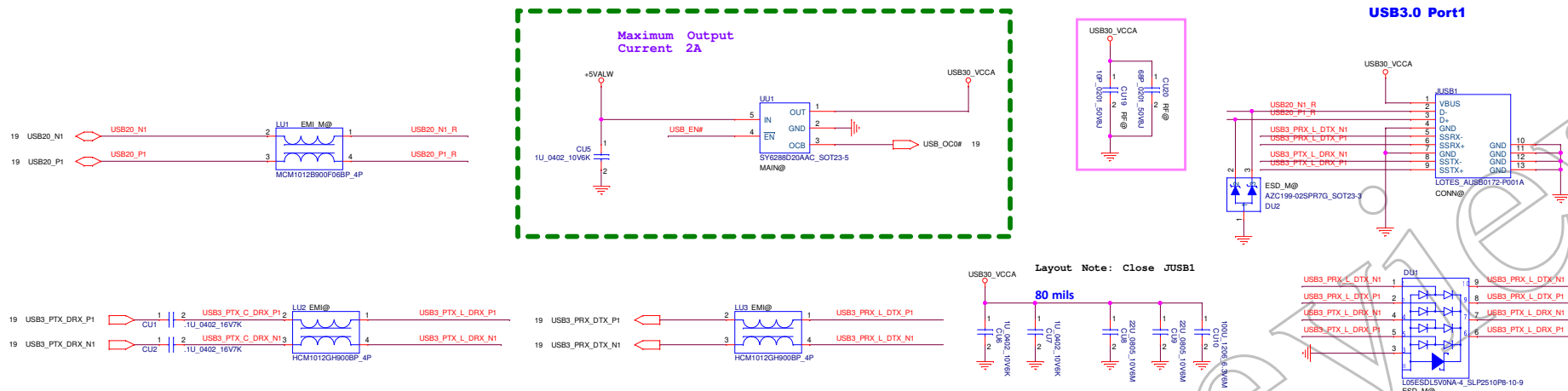


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								Size	Document Number			Rev	
								LA-F611P			0.3		
								Date: Thursday, March 22, 2018			Sheet 25 of 78		

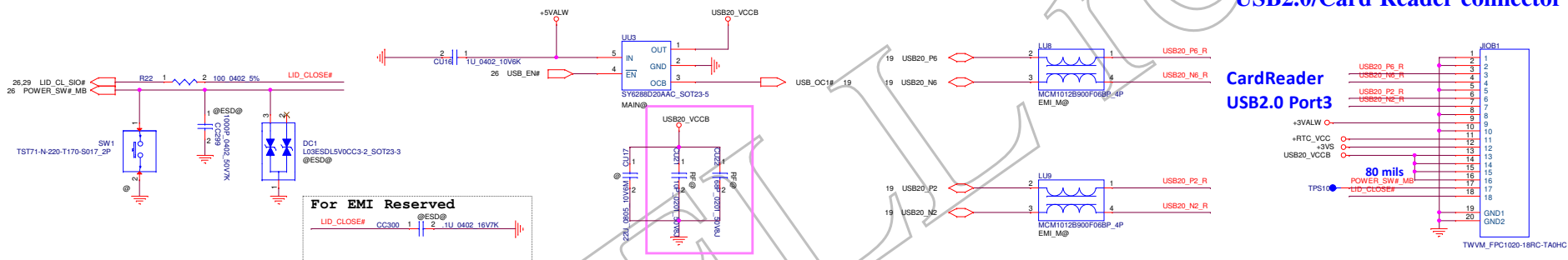
Main Func = EC



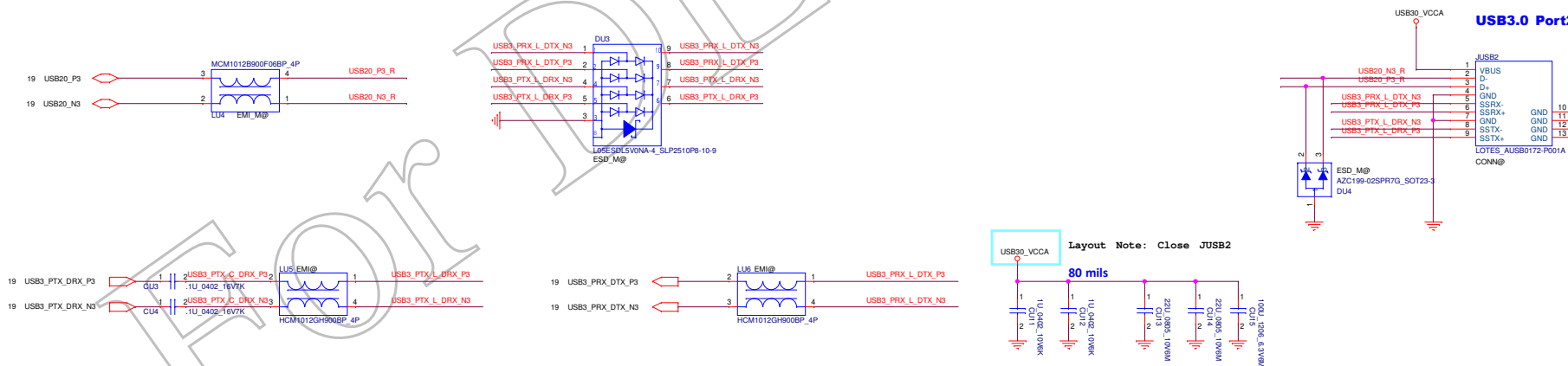
Main Func = USB3.0 Port1



Main Func = USB2.0 Port2 + Card Reader+Power BTN on IO/B

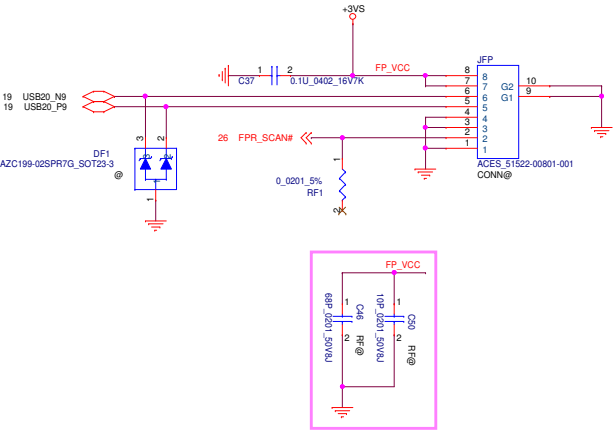


Main Func = USB3.0 Port2



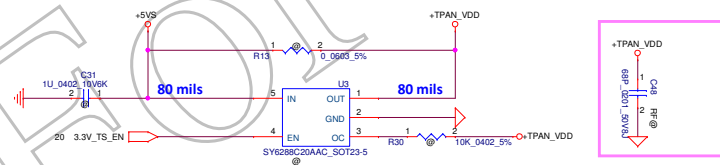
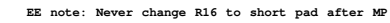
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	USB3.0 & I/O
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Main Func = Finger Printer



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Main Func = CAM



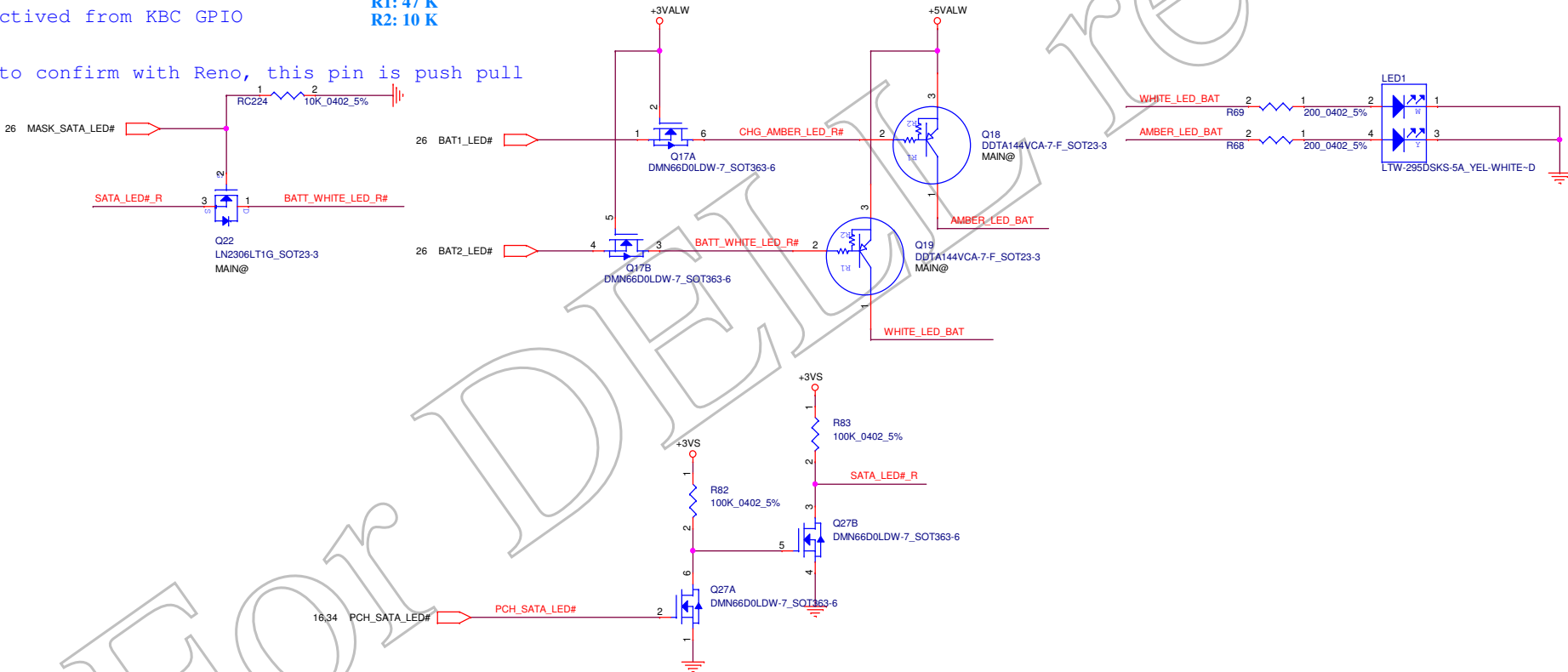
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	LCD/Camera/Mic
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Main Func = Battery LED

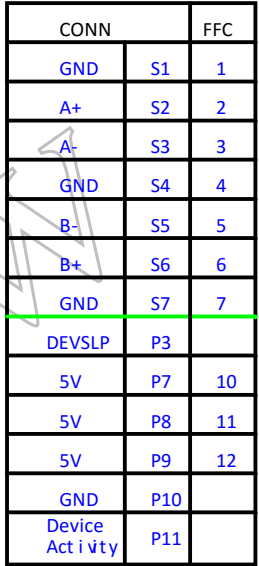
Low acted from KBC GPIO

Need to confirm with Reno, this pin is push pull

BJT
R1: 47 K
R2: 10 K

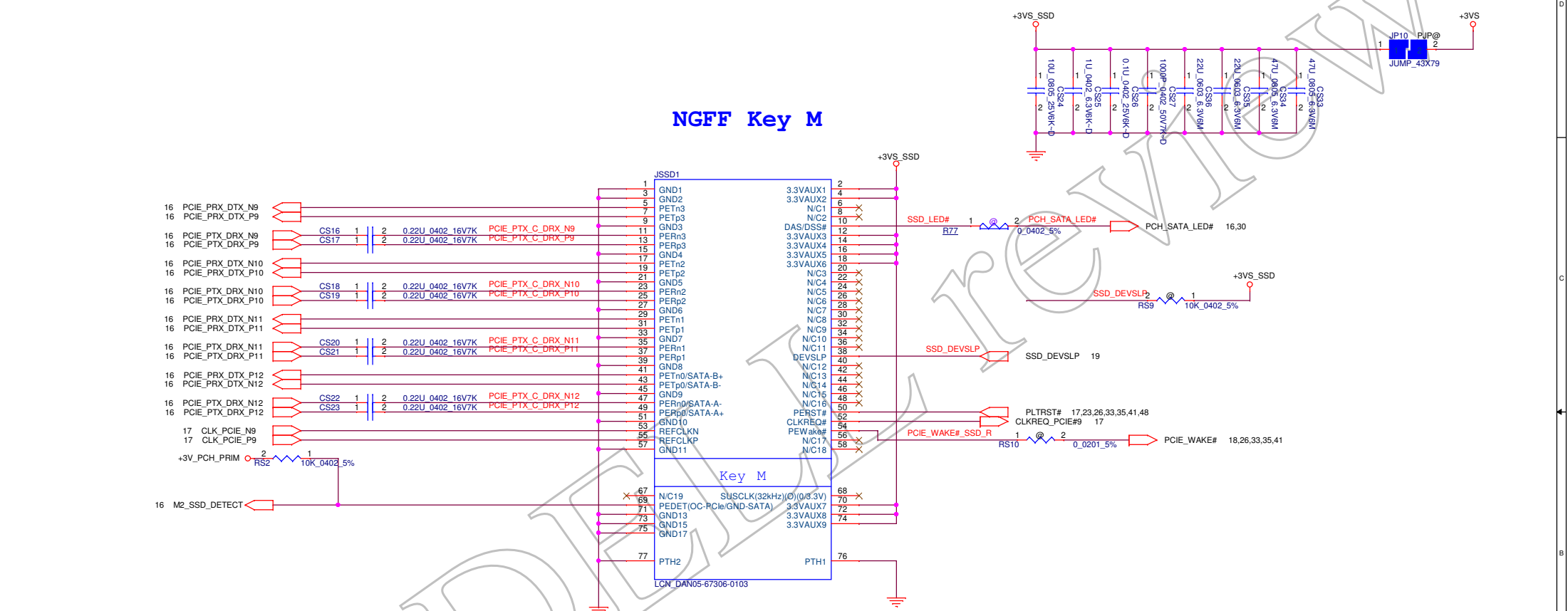


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				Size	Document Number
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				Size	Document Number	Rev
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Main Func = SSD
M Key CONN
Update OK



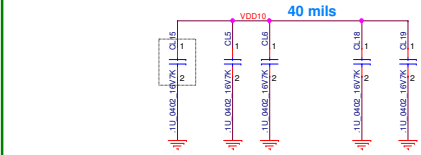
PEDET	Module Type
0	SATA
1	PCIe

LAN Chip (10/100/1000M & 10/100M co-layout)

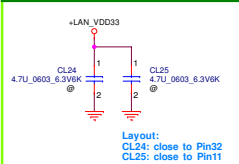
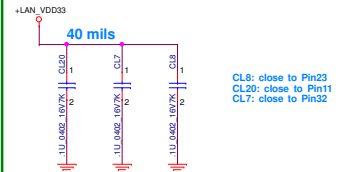
CL15, RL1:
Only for
RTL8111 LDO mode.

Layout:
For RTL8111H-CG
* Place CL5, CL6, CL18, CL19 close to each VDD10 pin 8, 30, 3, 22
For RTL8106E
* Place CL5, CL6 close to each VDD10 pin 8, 30

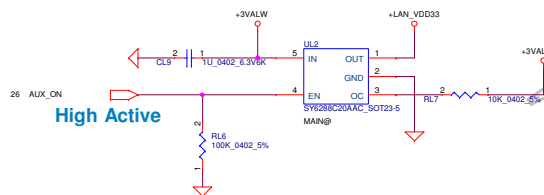
CL5: close to Pin8
CL6: close to Pin30
CL18: close to Pin3
CL19: close to Pin22



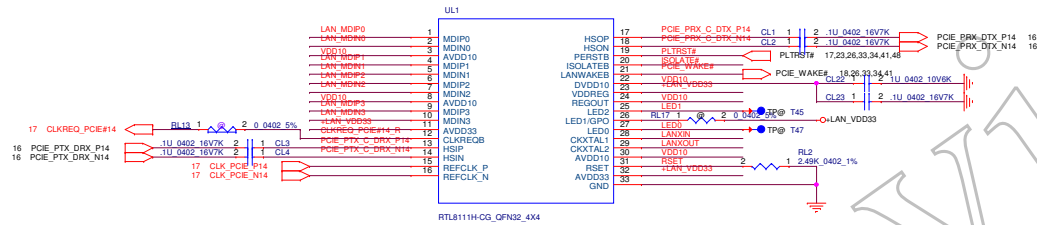
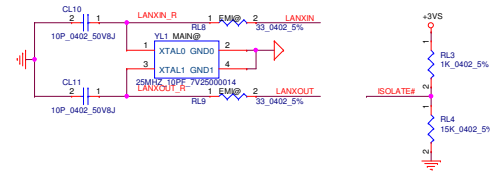
Layout:
For RTL8111H-CG
* Place CL20 and CL7 and CL8 close to each VDD33 pin 11, 32 ,23
For RTL8106E
* Place CL7 and CL8 close to each VDD33 pin 23, 32



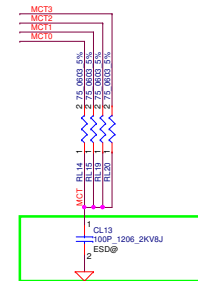
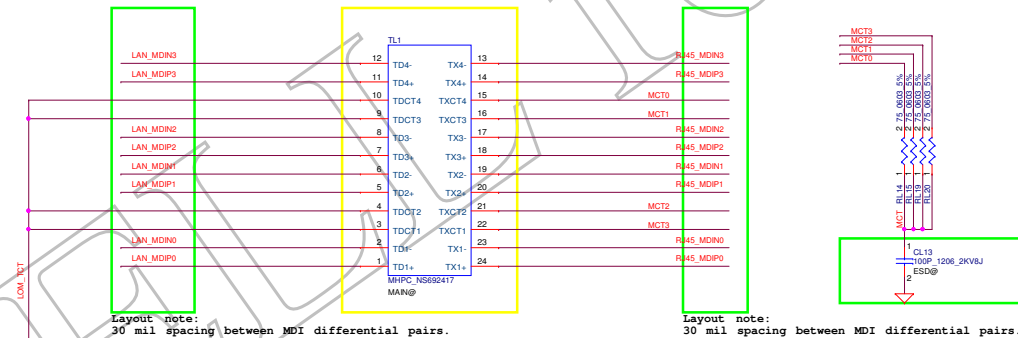
+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



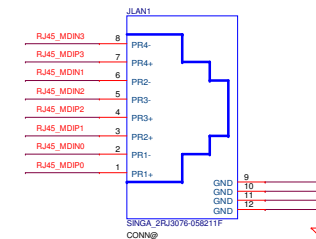
RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M



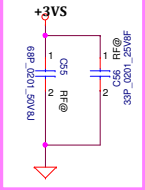
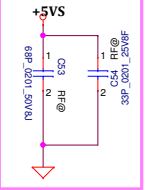
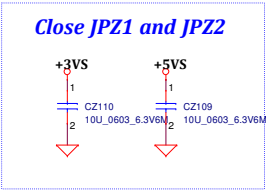
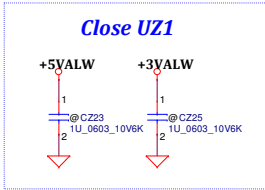
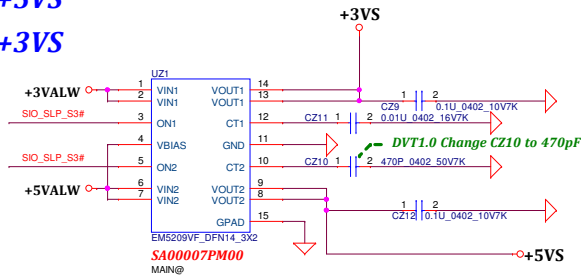
LAN TransFormer (10/100/1000M & 10/100M co-layout)



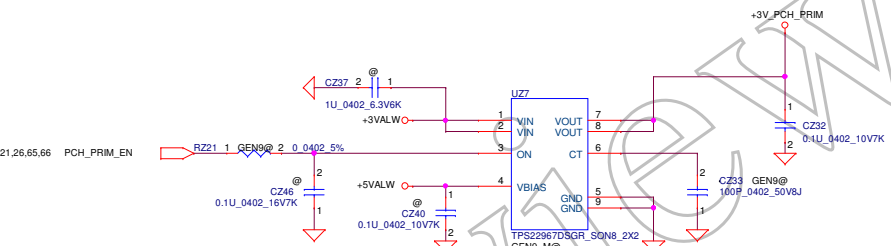
	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O



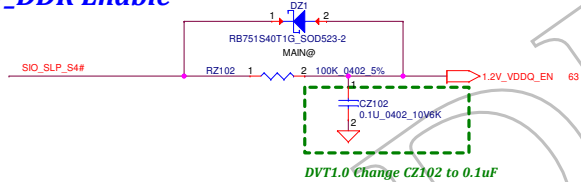
+5VALW to +5VS
+3VALW to +3VS



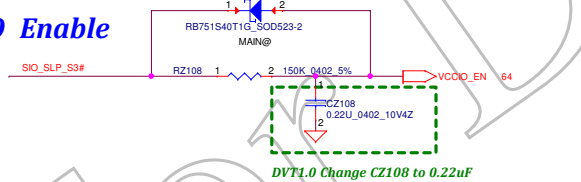
+3V_PCH_PRIM Load Switch



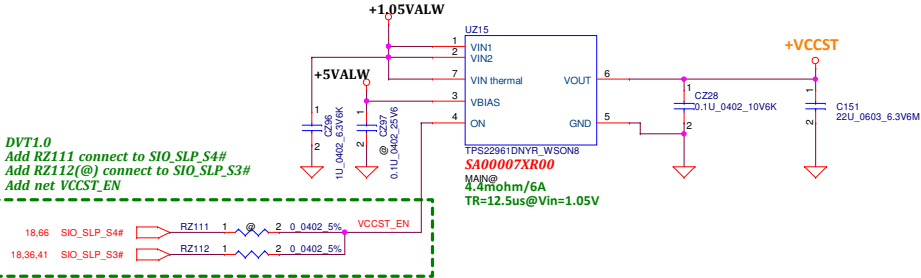
+1.2V_DDR Enable



+VCCIO Enable

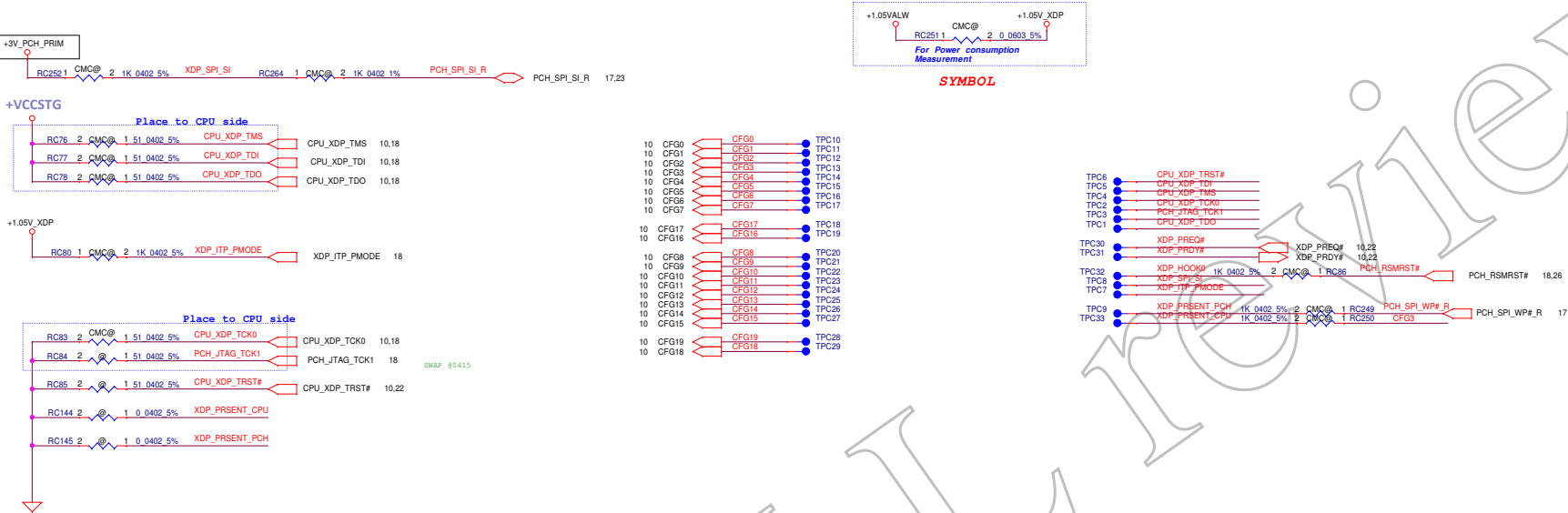


+VCCST Load Switch



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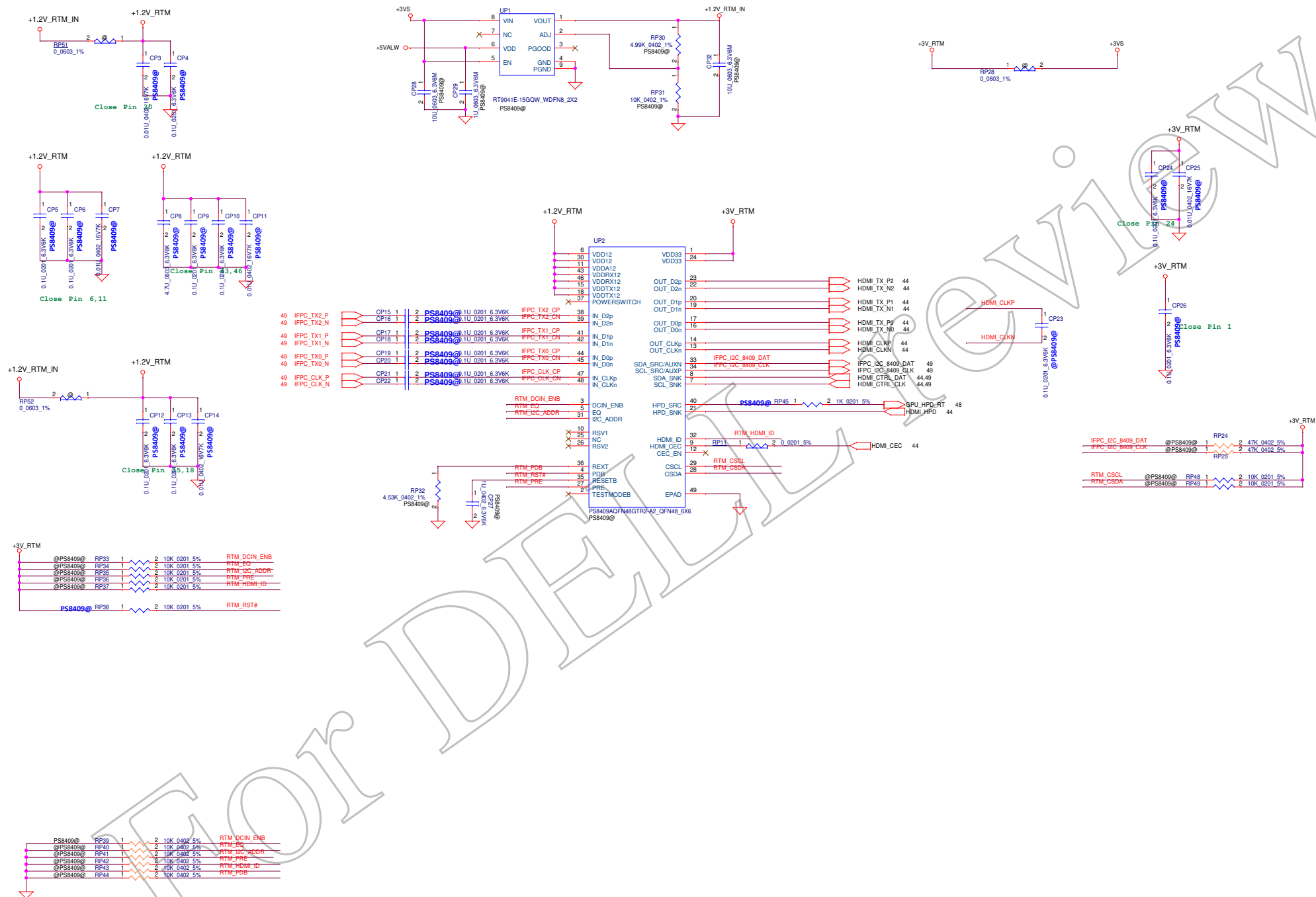
PRIMARY CMC CONN.



Reserved

For DELETED review

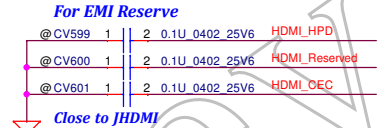
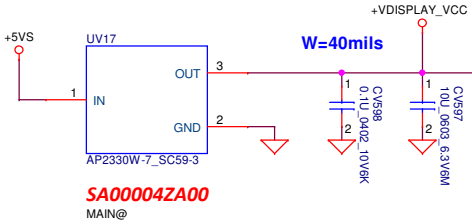
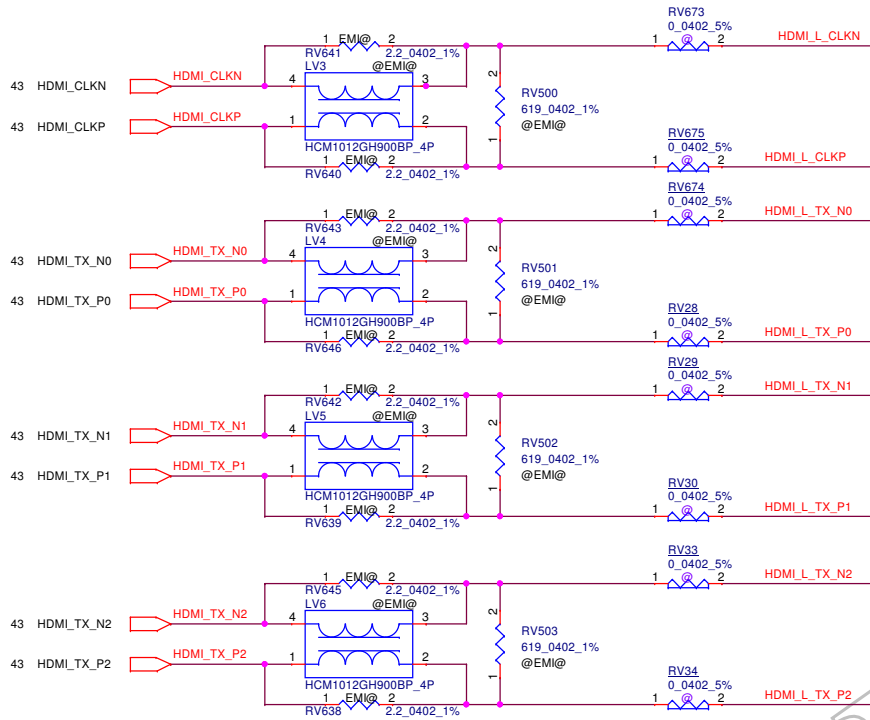
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Main Func = HDMI

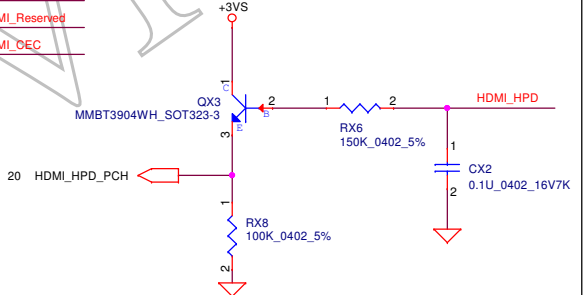
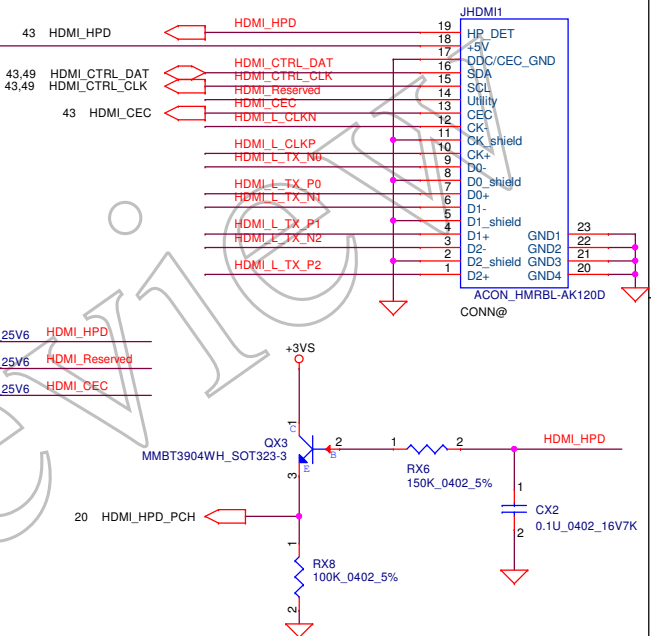
Place close to JHDMI1

HDMI conn



For EMI Reserve

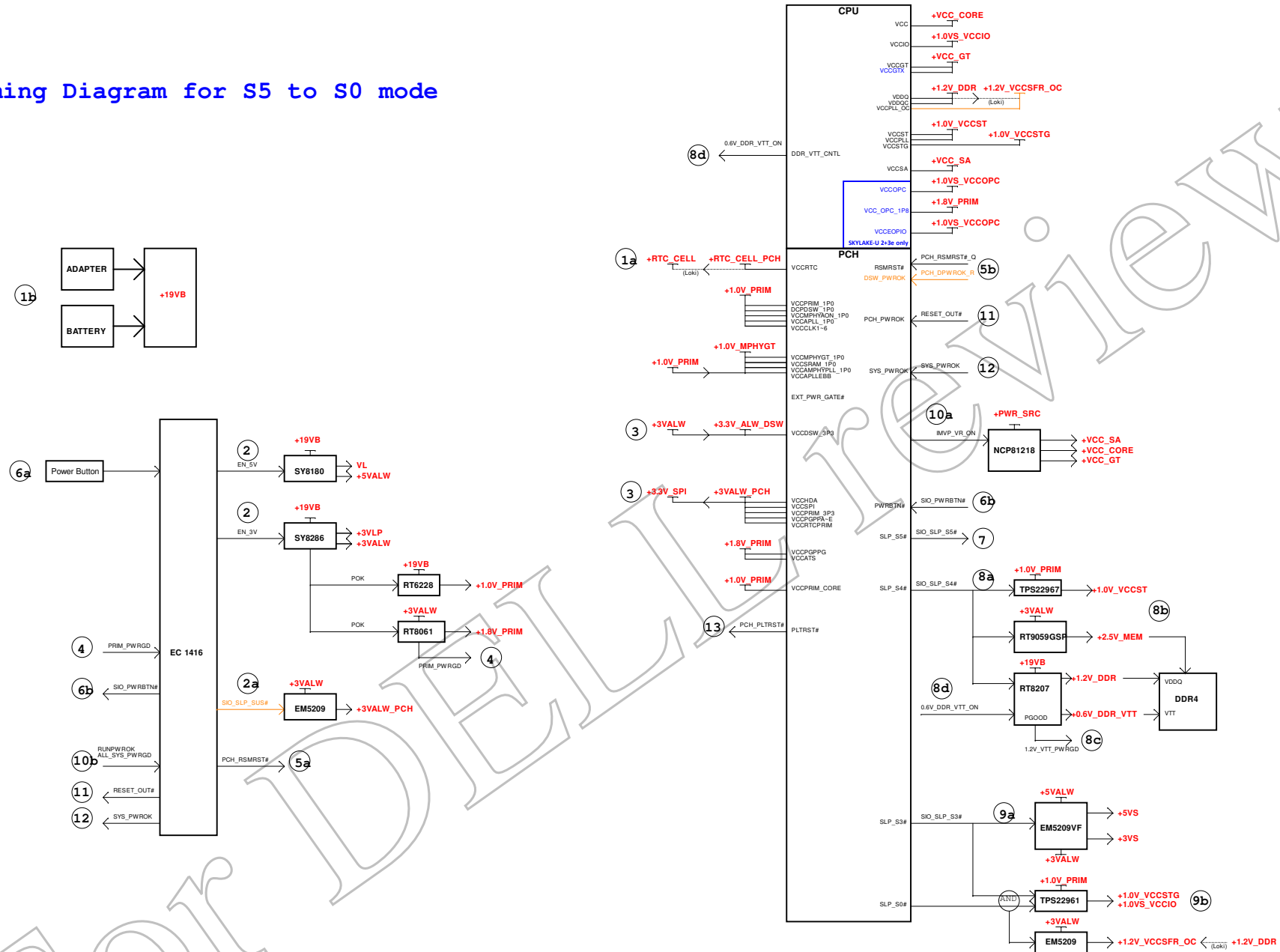
Close to JHDMI



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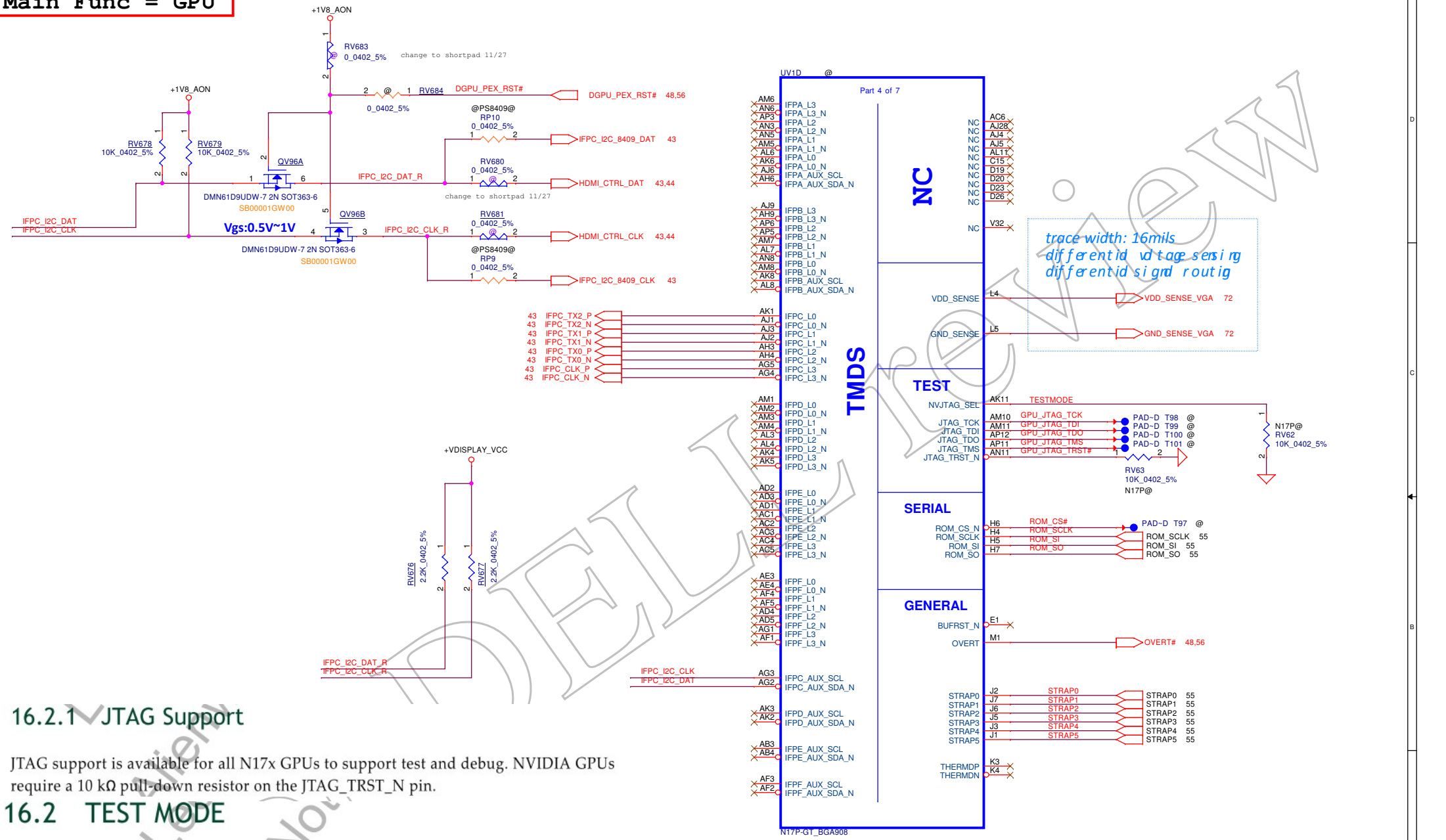
Timing Diagram for S5 to S0 mode



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				Date	Thursday, March 10, 2016
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Main Func = GPU



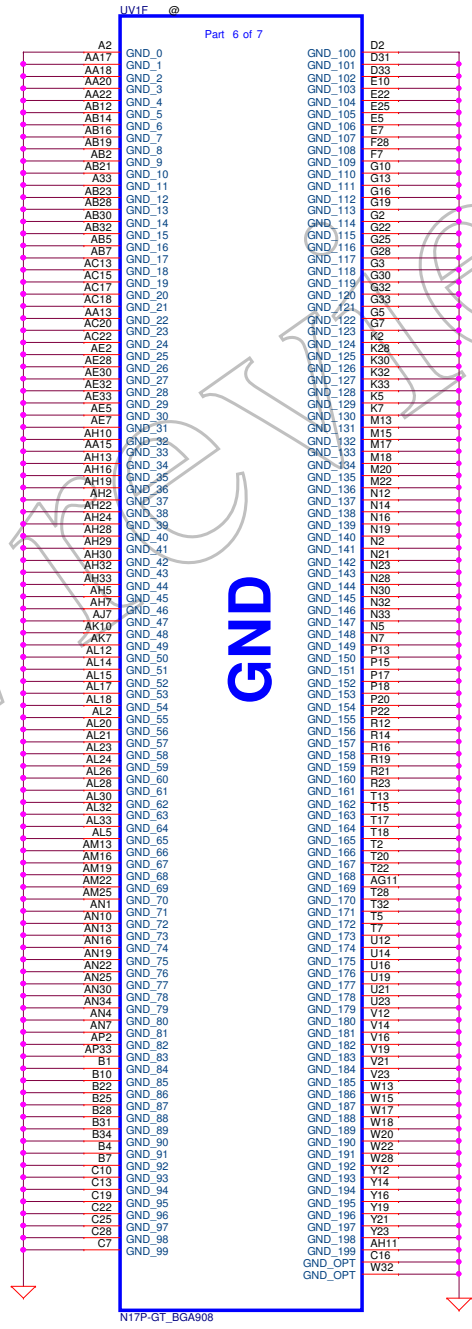
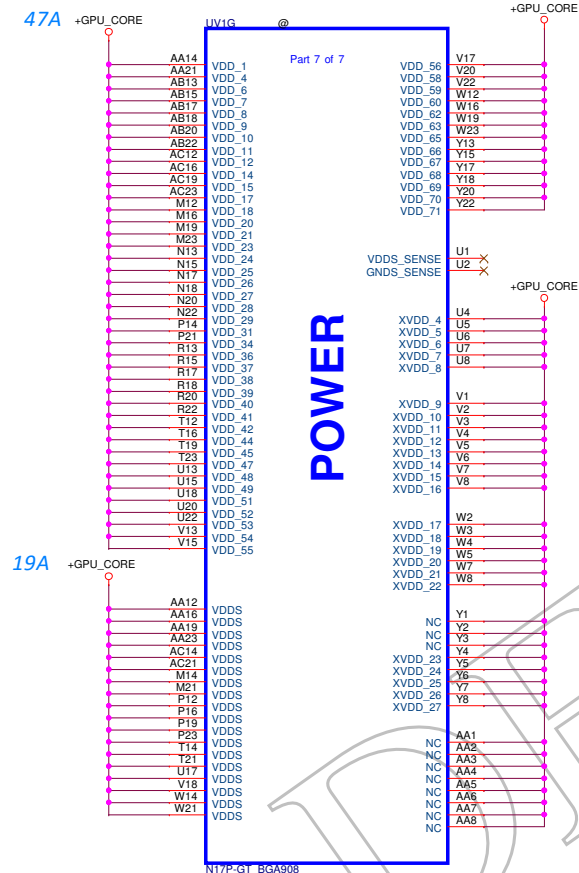
16.2.1 JTAG Support

JTAG support is available for all N17x GPUs to support test and debug. NVIDIA GPUs require a 10 kΩ pull-down resistor on the JTAG_TRST_N pin.

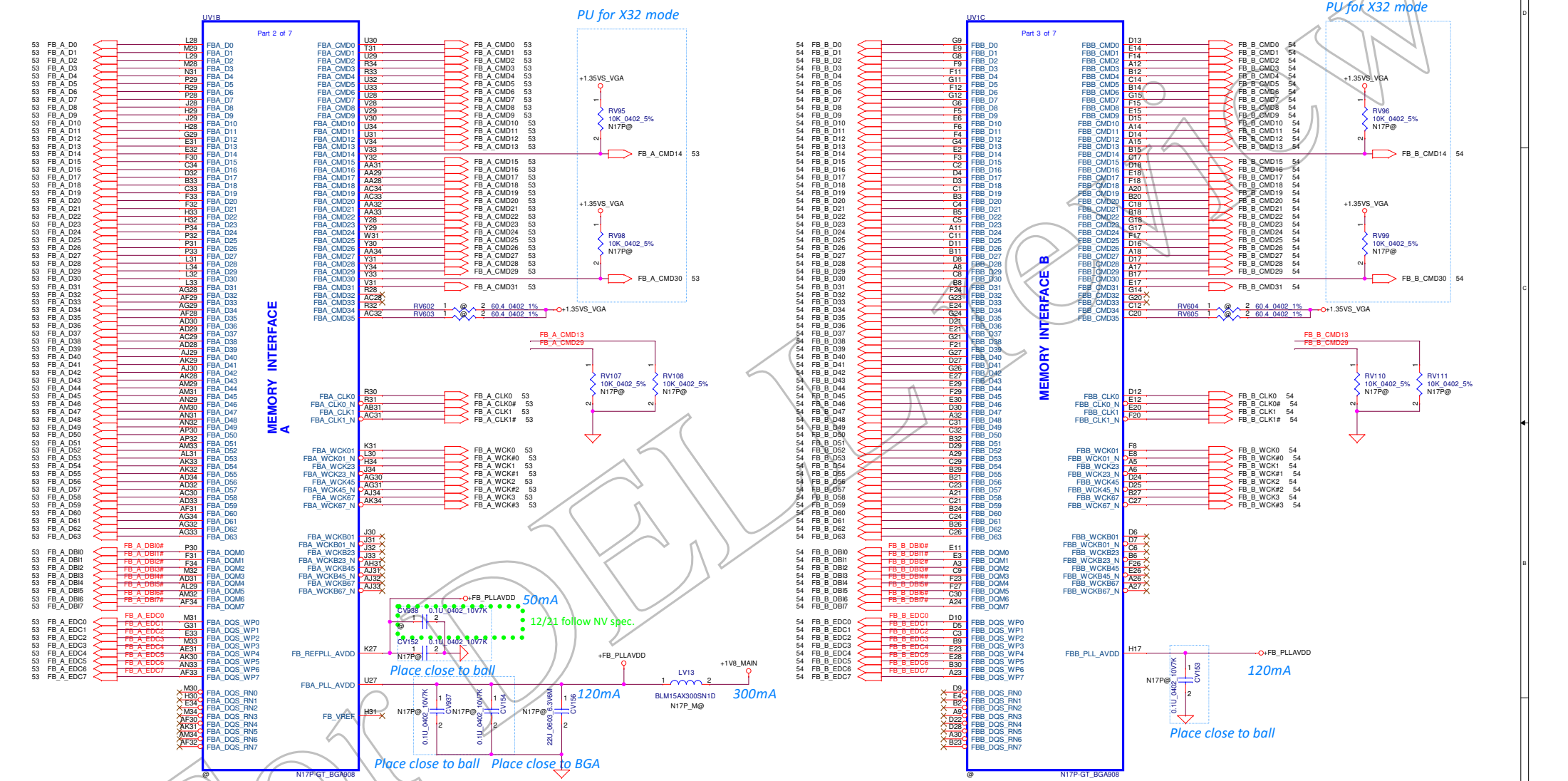
16.2 TEST MODE

By default, pull-down the TESTMODE pin (pin name is NVJTAG_SEL in some N17x pinouts) to GND with a 10 kΩ resistor. For ICT/boundary scan requirements, contact your NVIDIA AE.

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Size		Document Number		Rev	
		LA-F611P		0.3	
Date:		Thursday, March 22, 2018		Sheet 49 of 78	

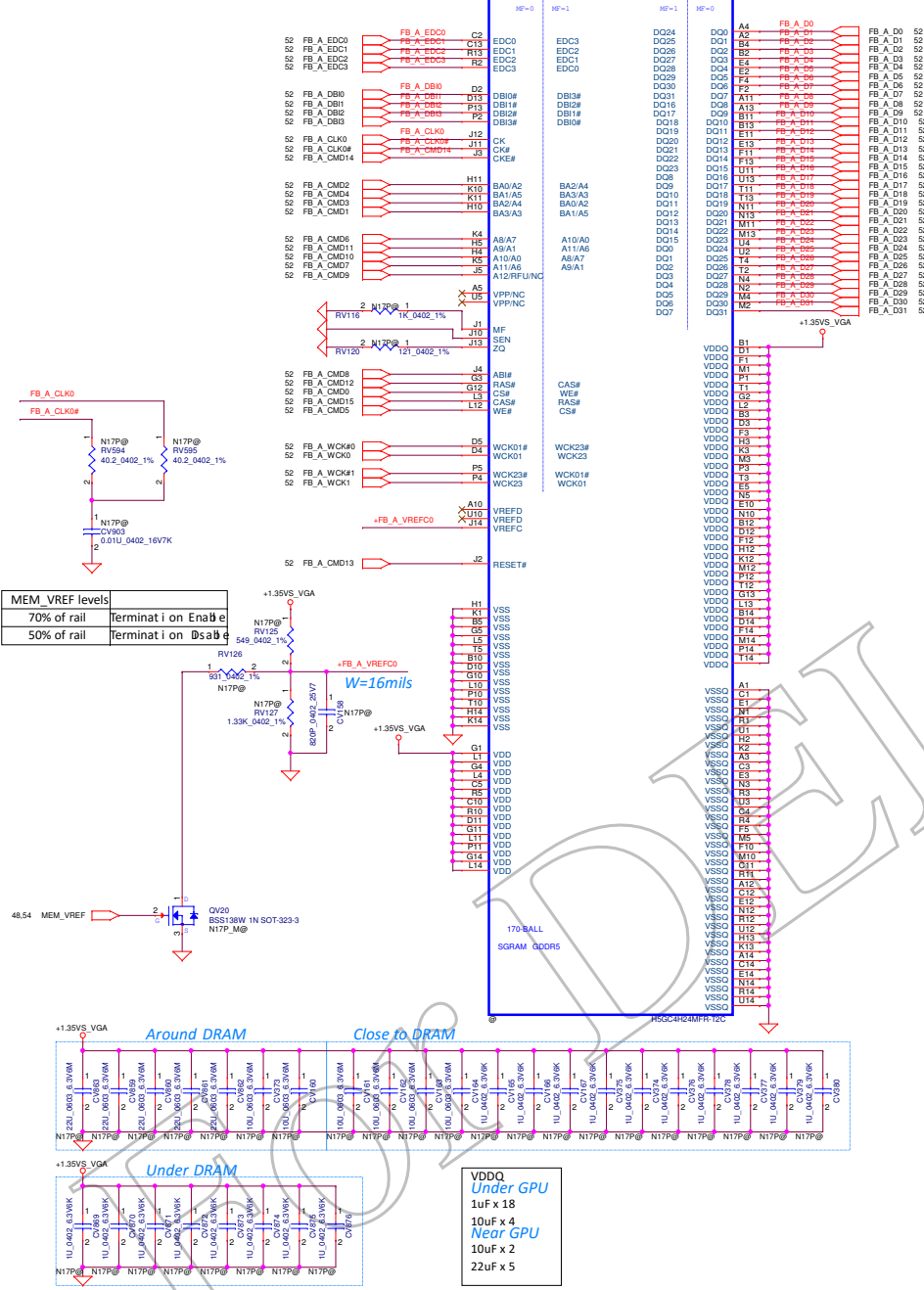


Main Func = GPU

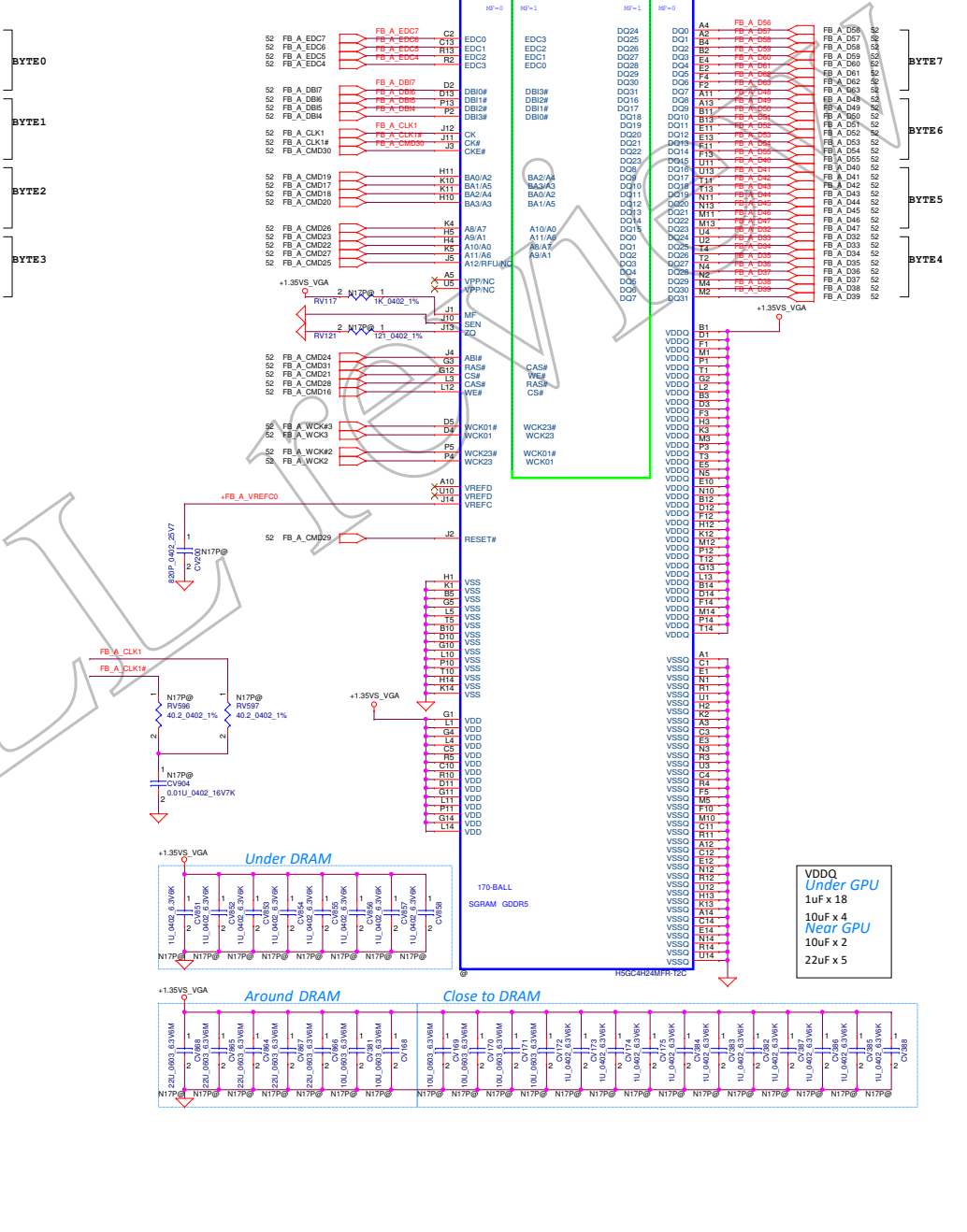


Memory Partition A- Lower 32 bit

MF=0



MF=1



Memory Partition A- Lower 32bit

MF=0

MF=1

MF=2

MF=3

MF=4

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MF=6

MF=7

MF=8

MF=9

MF=10

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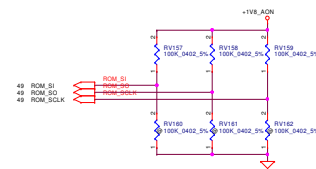
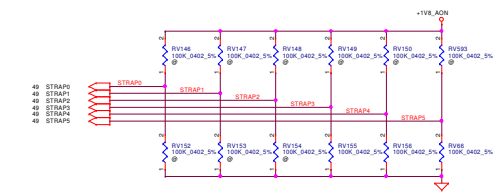


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins			See Note				Resulting SORx_EXPOSED Enablements			
	ROM_SI	ROM_SO	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED				
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED				
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled				
13	L	L	L	ENABLED	ENABLED	disabled	ENABLED				
12	L	H	H	ENABLED	ENABLED	disabled	disabled				
11	H	H	H	ENABLED	disabled	disabled	disabled				
0	H	H	M	disabled	disabled	disabled	disabled				
	M	X	X	(Reserved; do not configure)							
All other Strap Configurations				(Reserved)							

All other Strap Configurations (Reserved)

Table 5.2 RAMCFG

Strap Pins <small>See Note</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins ^{Note 1}			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

Table 3. N17P-G0/-G1 GD0R5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/V	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed (MHz)	Date Code	Qual Plan	Status
8 Gb	2666x32	1.35V and 1.5V ¹	Samsung	K4G803237B-HC28	B-die	0x0	1066	N/A	Full	Production ready
			Samsung	K4G803237B-HC25	B-die	0x0	1066	N/A	Full	Substitution allowed with wafer
			Micro	MT71256832HF-70-A	A-die	0x1	1066	N/A	Full	Production ready
			Micro	MT71256832HF-70-A	A-die	0x1	1066	N/A	Full	Substitution allowed with wafer
			Hynix	H5GCH42ALR-RAC	M-die	0x2	1066	N/A	Full	Post production ready
			Hynix	H5GCH42ALR-RAC	M-die	0x2	1066	N/A	Full	Substitution allowed with wafer
4 Gb	1286x32	1.35V and 1.5V ¹	Samsung	K4G41237B-HC28	B-die	0x7	1066	N/A	Full	Production ready
			Samsung	K4G41237B-HC25	B-die	0x7	1066	N/A	Full	Substitution allowed with wafer
			Hynix	H5GCH42ALR-RAC	A-die	0x4	1066	N/A	Full	Production ready
			Hynix	H5GCH42ALR-RAC	A-die	0x4	1066	N/A	Full	Substitution allowed with wafer

SMB_ALT_ADDR	Single GPU
Low	High
DEVID_SEL	Original Device ID
Low	High
VGA_DEVICE	3D Device
Low	High
PCIE_CFG	Normal signal swing
Low	High
	Reduce the signal amplitude

ROM_SI	ROM_SO	ROM_SCLK	STRAP5	STRAP4	STRAP3	STRAP2	STRAP1	STRAP0
H	H	H	L	L	L	L	L	L
IFPA	IFPB	IFPC	IFPD (eDP only)	IFPE	IFPF			
NA	NA	HDMI	NA	NA	NA	NA	NA	NA

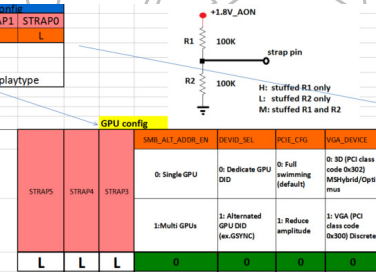
ROM_SI	ROM_SO	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
H	H	H	Enable	Disable	Disable	Disable

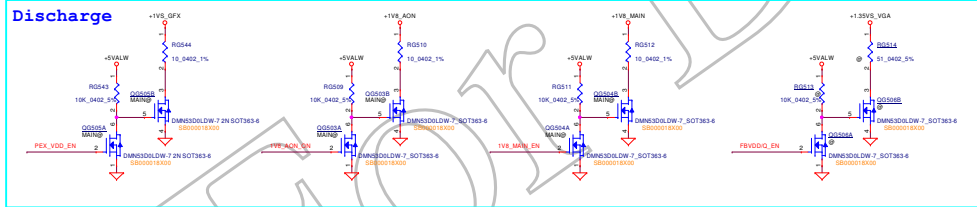
Display Link to SORx_EXPOSED Mapping for Down Designs			
Total Display Links (HDMI, DP or DVI)	See This Row of Table 3.5	Is IFPD used? (Only supports eDP.)	See This Row of Table 3.5
4	4	NO	15
4	3	YES	13
3	3	NO	14
3	2	YES	12
3	2	NO	10
2	1	YES	9
1	1	NO	8
1	0	YES	6

No other configurations are supported.

Select your display config

8





Timing diagram for the PE_FIBEN signal. The diagram shows the relationship between FE_CBE, PE_FIBEN, GPU_FIBEN, GPU_FIBEN*, IYS_MNEN, All Rail P000, and GPU_FIBEN* over time. PE_FIBEN is active (low) during the Self-Burnish phase, which occurs after FE_CBE transitions from Normal to Self-Burnish and before it returns to Normal. GPU_FIBEN and GPU_FIBEN* are active during the Self-Burnish phase. IYS_MNEN is active during the Self-Burnish phase. All Rail P000 is active during the Self-Burnish phase. GPU_FIBEN* is active during the Self-Burnish phase.

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN# EN assertion to all power rails up and stable	0.04	4	ms

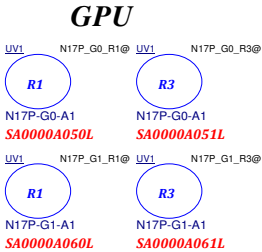
[illegible]

Timing diagram showing the relationship between PEK_RST# and GPU_FWR_EN signals. The diagram illustrates two transitions: T0 (GPU power off) and T1 (GPU power on). PEK_RST# is active-low, and GPU_FWR_EN is active-high. The M/Rail PGCOD and PGIE_Link signals are also shown, with PGIE_Link having a high impedance state (X) during the power transitions.

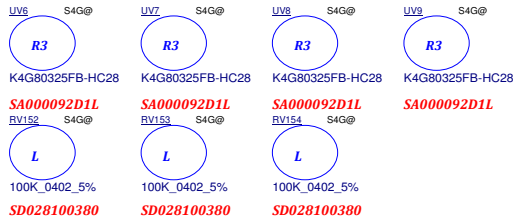
Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

MODEL NAME : CALXX/CALXX
PCB NO : LA-F611P

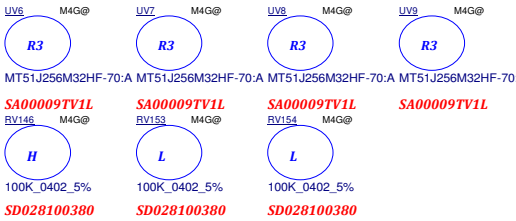
Bom
Structure



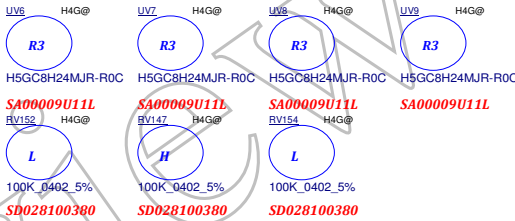
X76 : S4G@ X76XXXXXLXX
Samsung 4G



X76 : M4G@ X76XXXXXLXX
Micron 4G



X76 : H4G@ X76XXXXXLXX
Hynix 4G



Samsung 4G

Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
0	L	L	L

Micron 4G

Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
1	L	L	H

Hynix 4G

Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
2	L	H	L

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V ²	Samsung	K4G80325FB-HC28	B-die	0x0	Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	Gbps	N/A	N/A	Substitution allowed with waiver ¹
			Micron	MT51J256M32HF-70A	A-die	0x1	Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80A	A-die	0x1	Gbps	N/A	N/A	Substitution allowed with waiver ¹
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24MJR-R4C	M-die	0x2	Gbps	N/A	N/A	Substitution allowed with waiver ¹
4 Gb	128Mx32	1.35V and 1.5V ²	Samsung	K4G41325FE-HC28	E-die	0x7	Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	Gbps	N/A	N/A	Substitution allowed with waiver ¹
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	Gbps	N/A	Full	Production ready
			Hynix	H5GC4H24AJR-R4C	A-die	0x6	Gbps	N/A	N/A	Substitution allowed with waiver ¹
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
		1.35V and 1.55V ¹	Micron	EDW40328ABG-70-F	A-die	0x8	Gbps	N/A	Full	Post production ready

For DELL review

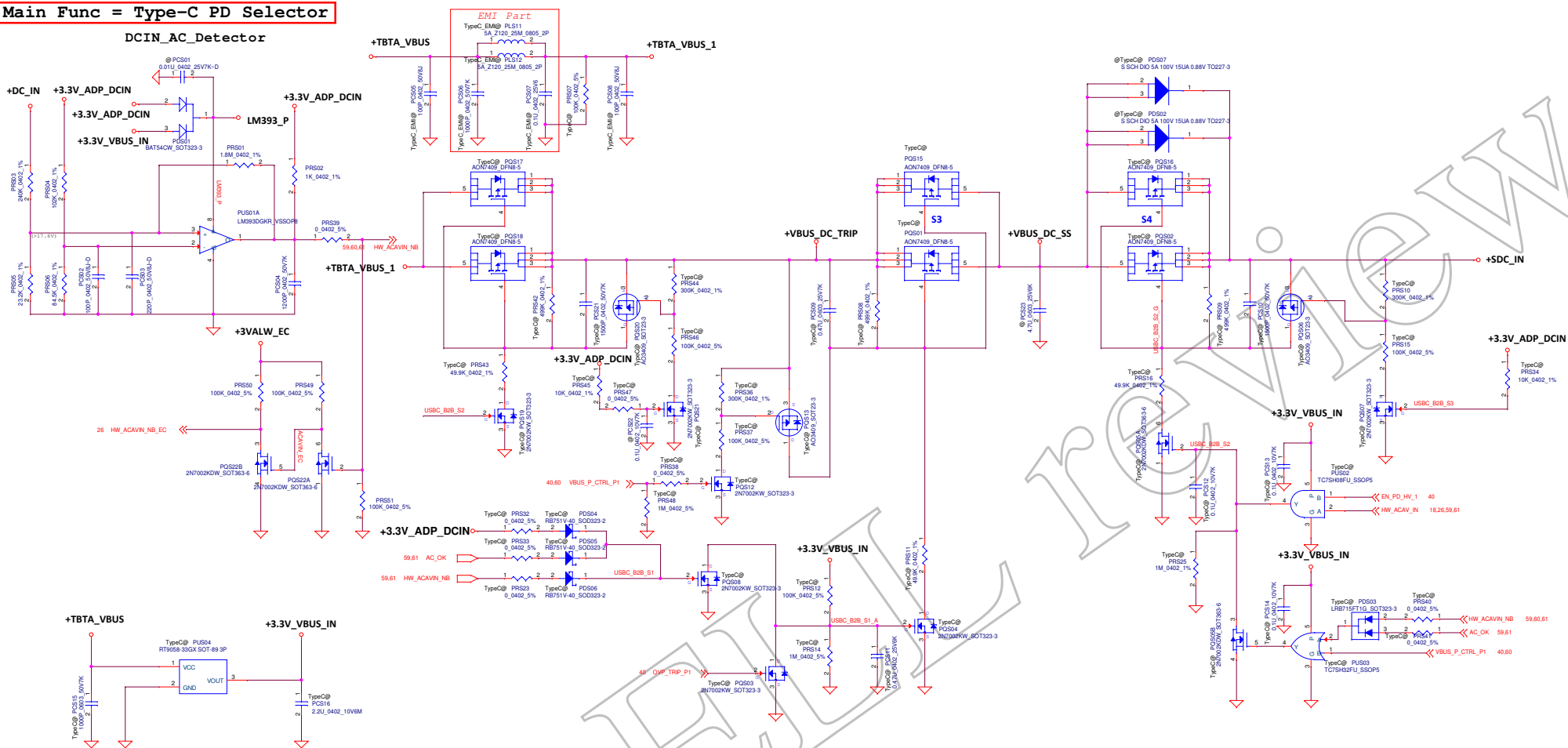
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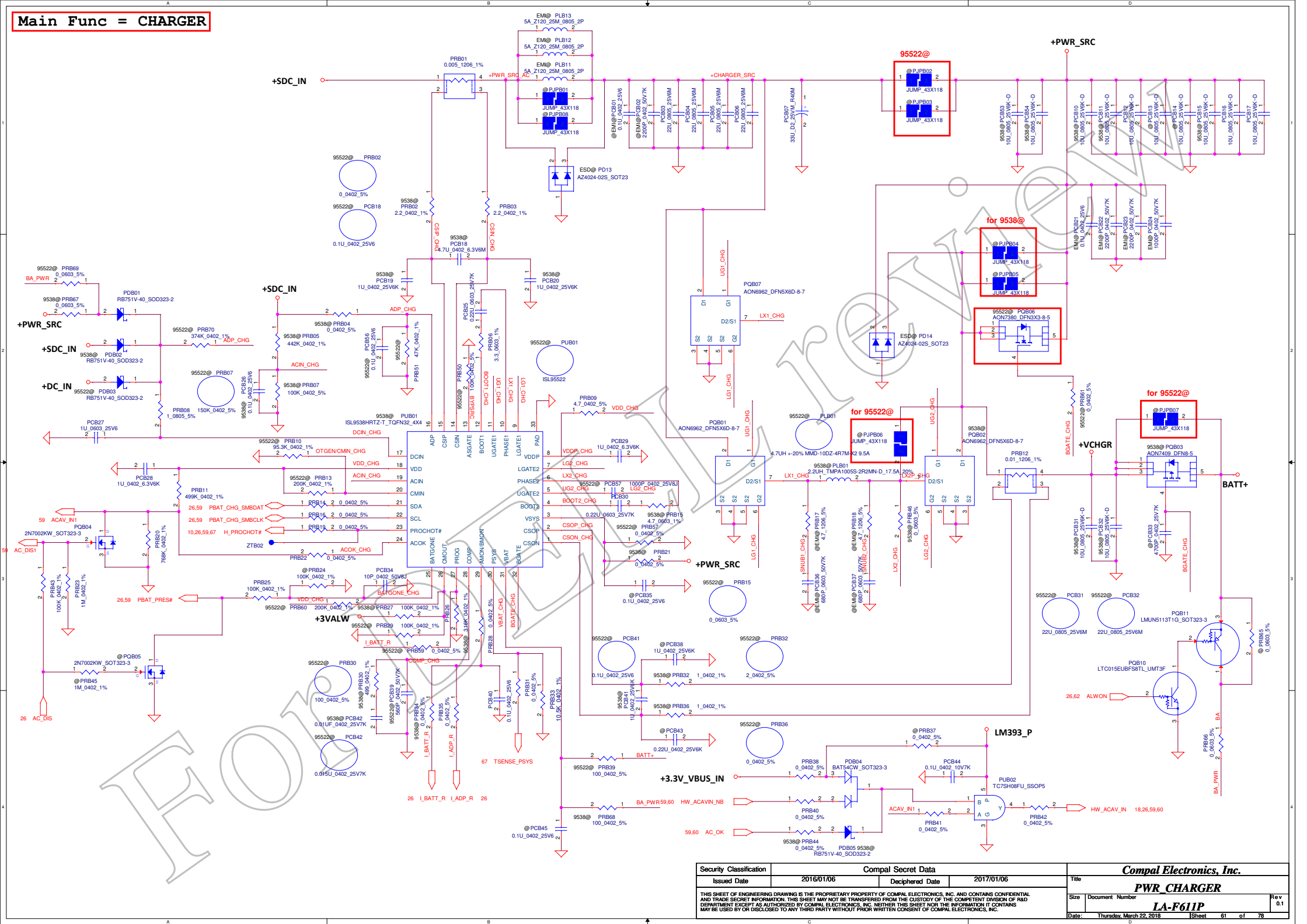
Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR DCIN/BATT CONN LA-F611P	
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Main Func = Type-C PD Selector



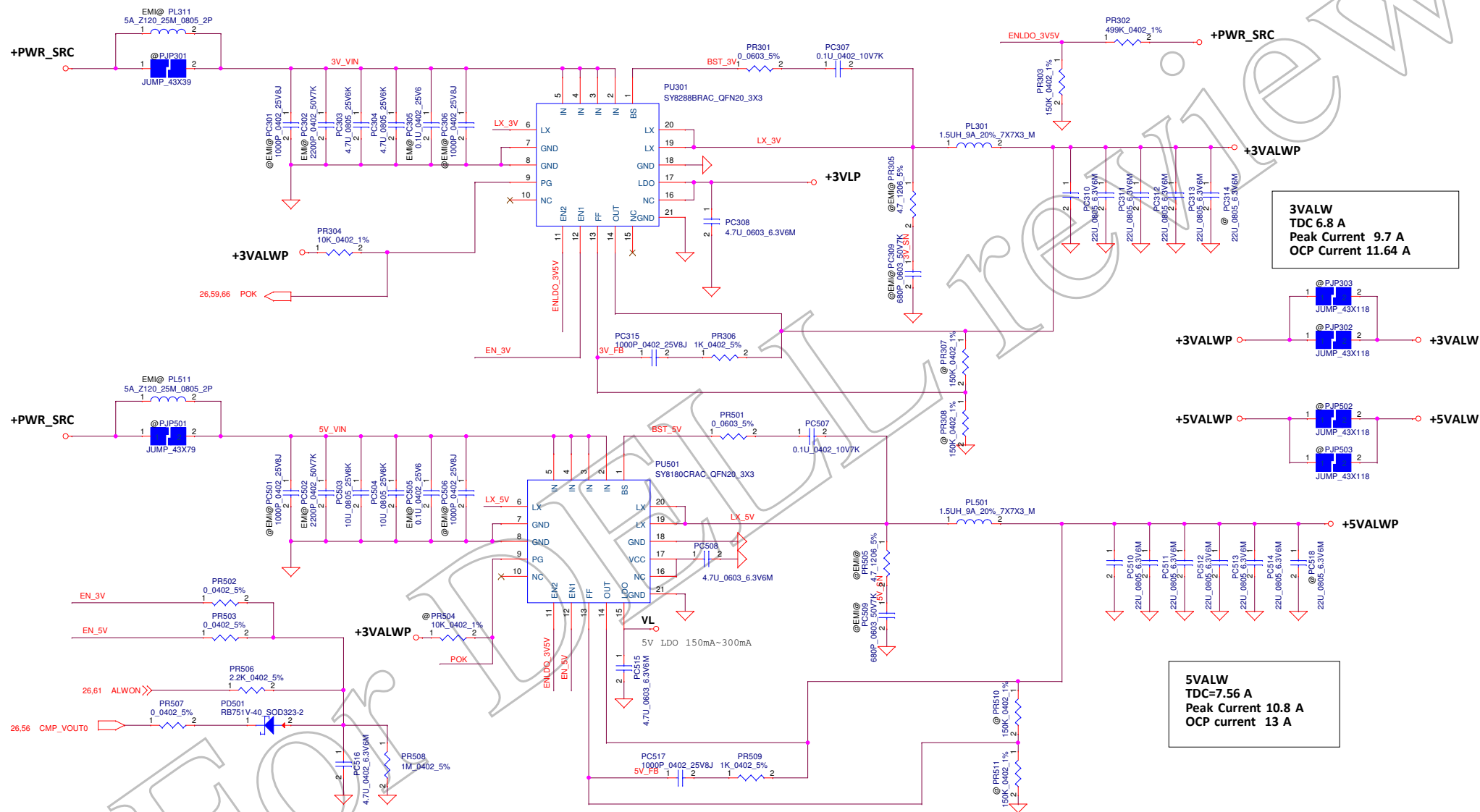
Security Classification	Compel Secret Data		Title		Compel Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Size		Document Number
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Main Func = CHARGER



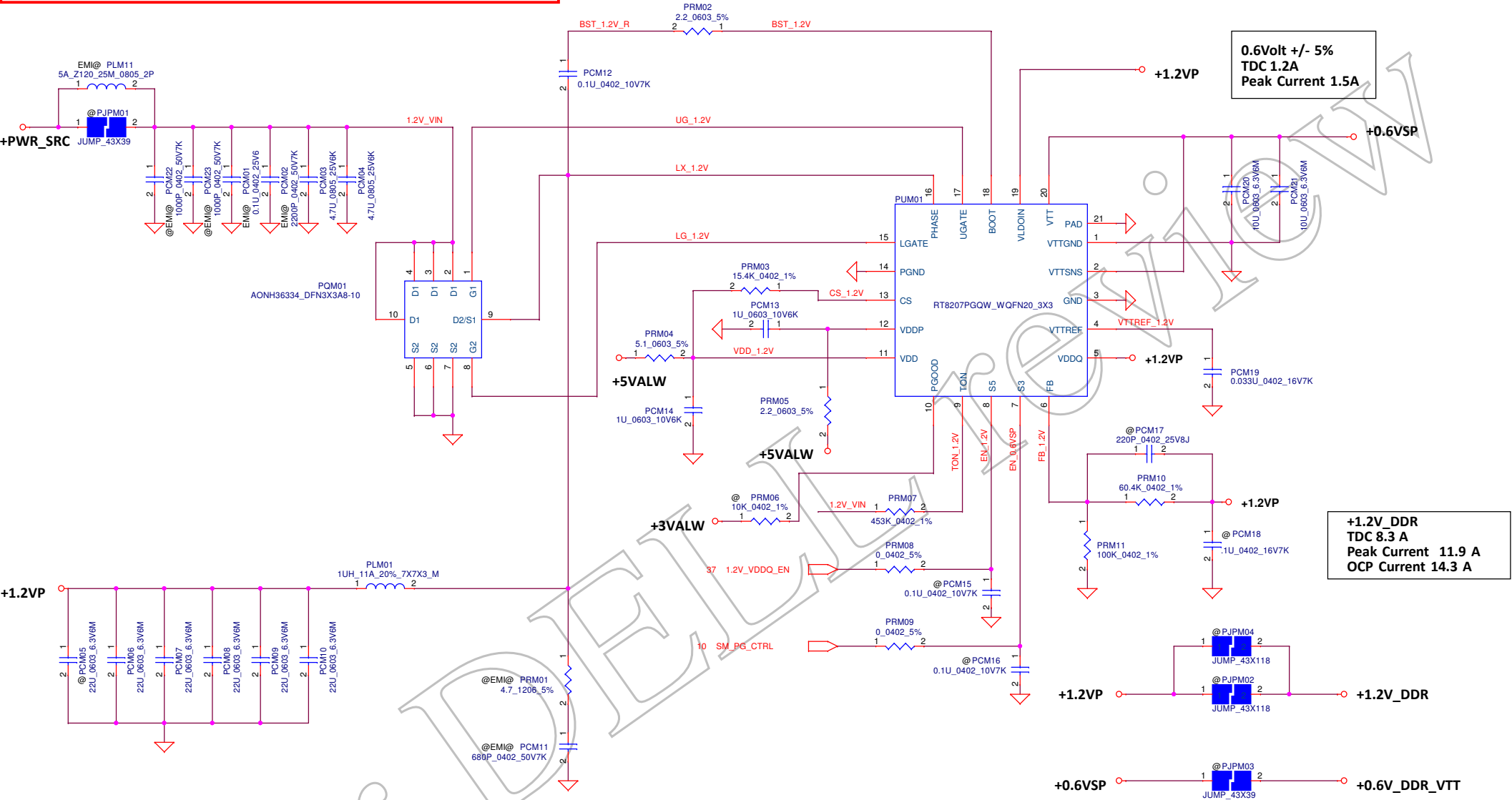
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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Main Func = 3.3VALW/5VALW



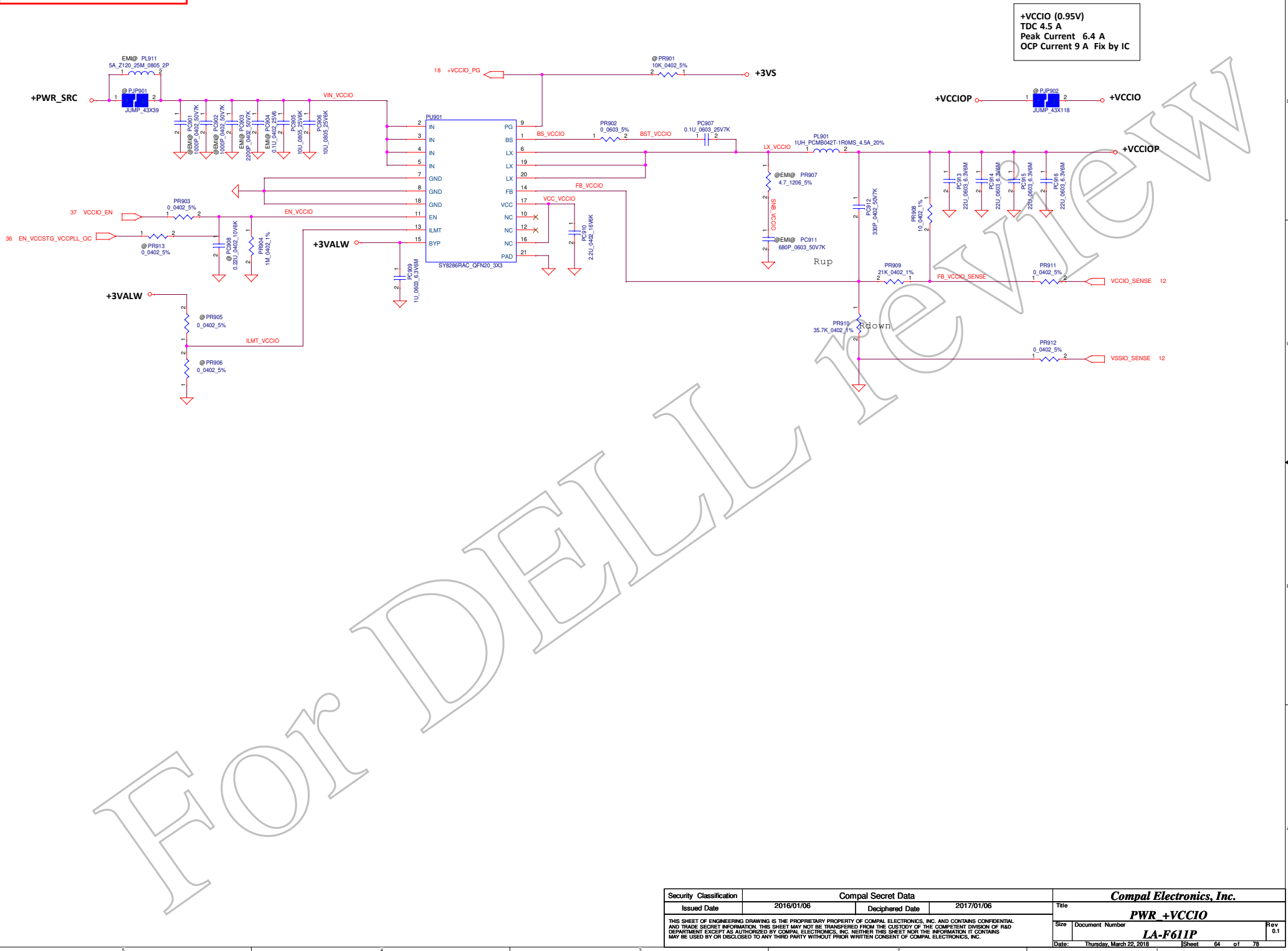
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2016/01/06	Deciphered Date	2017/01/06	Title		
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Main Func = 1.2V_DDR/+0.6V_DDR_VTT



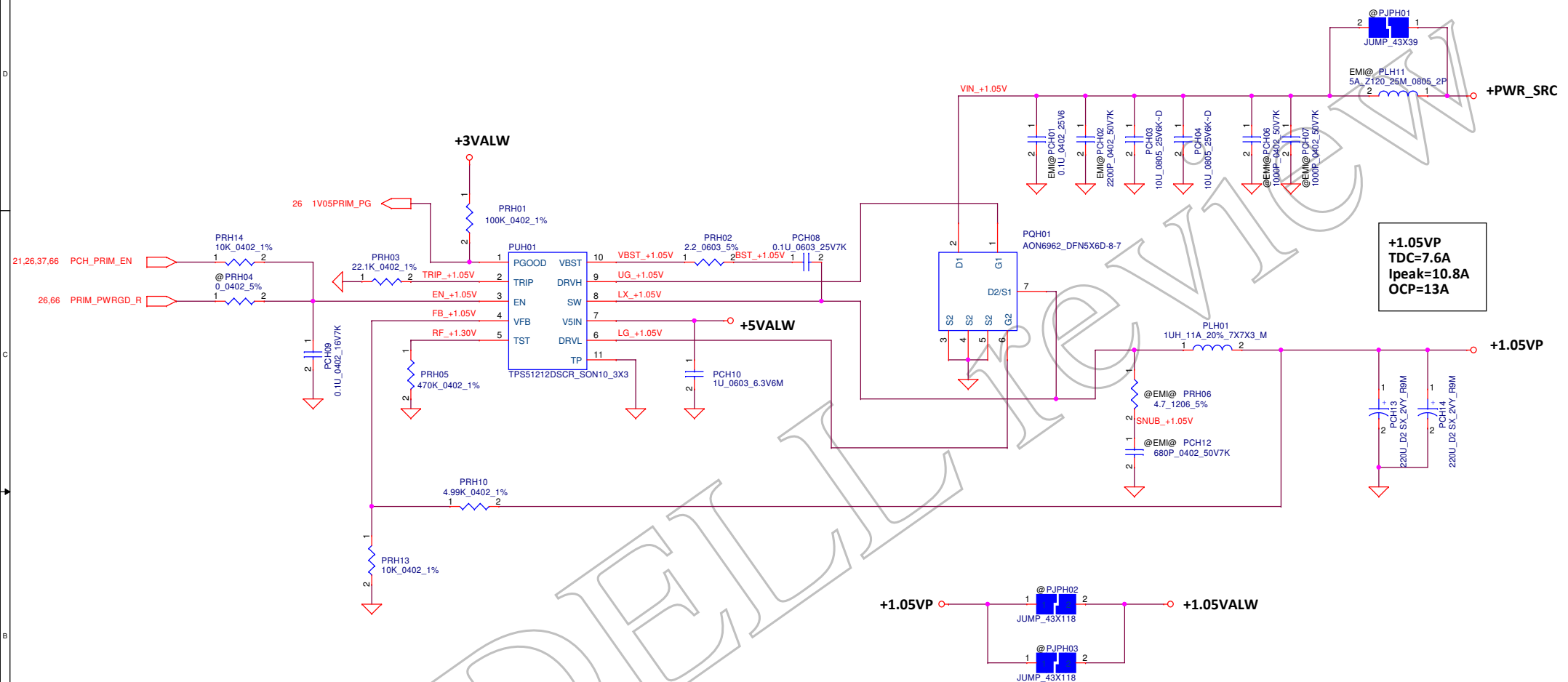
Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR +1.2V DDR/+0.6V DDR VTT	
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Main Func = VCCIO



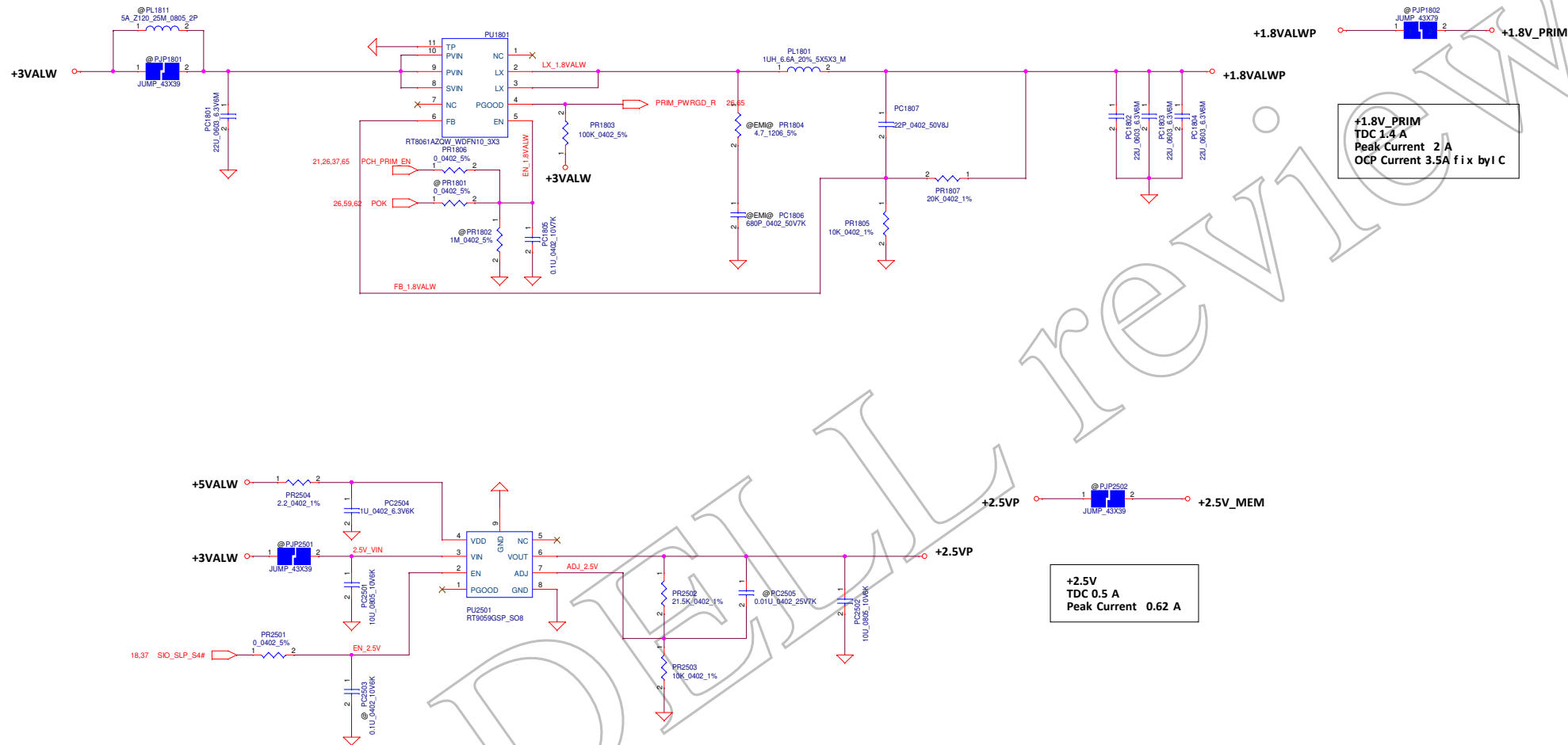
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Main Func = 1.05VALW



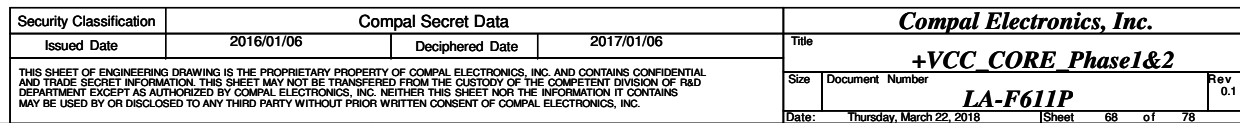
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Main Func = +1.8V_PRIM/+2.5V_MEM

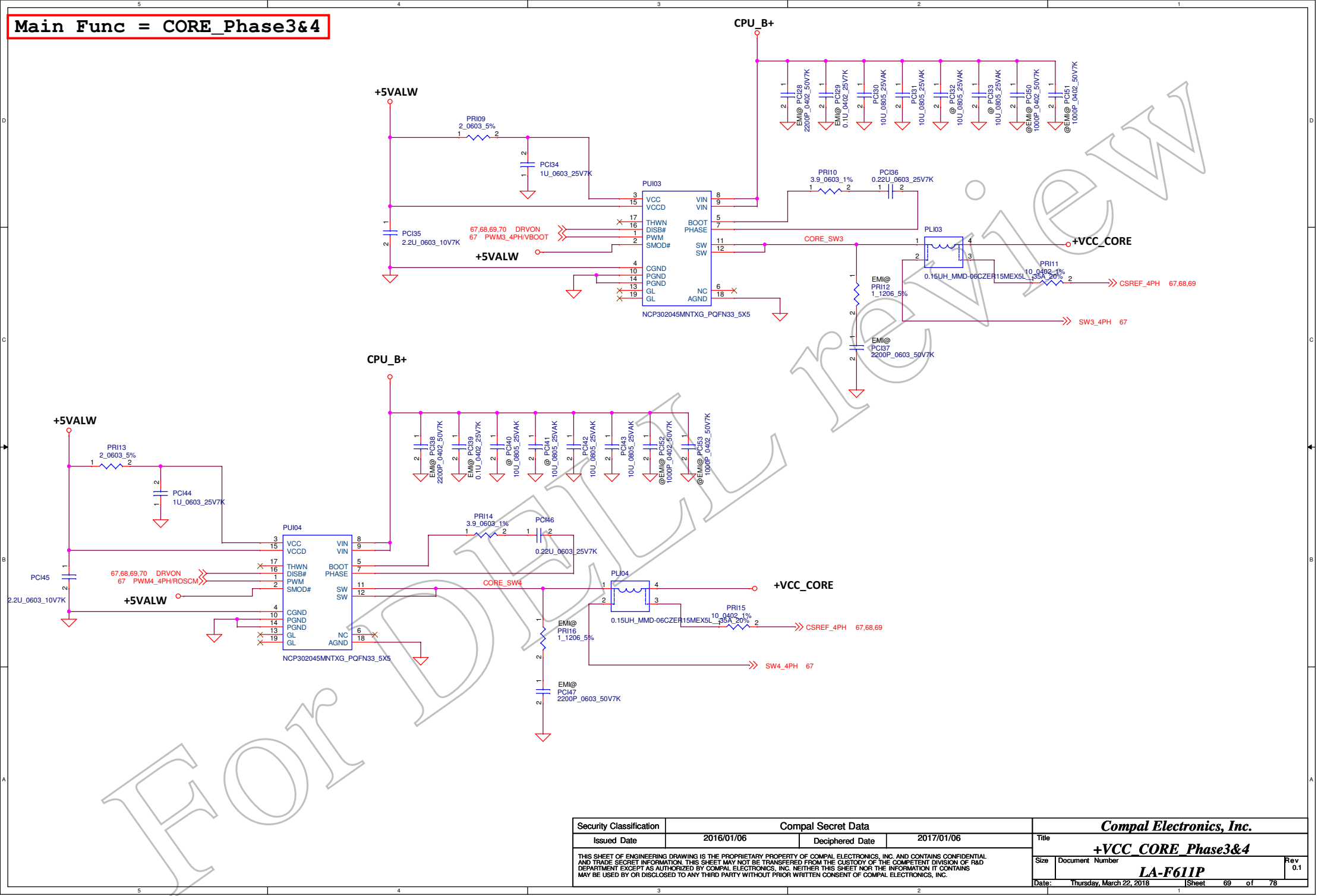


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+VCC_CORE
TDC PL2 :80A
Peak Current 128A
OCP Current 154A
DCR 0.9mohm +/-5%
Load Line 1.8mV/A



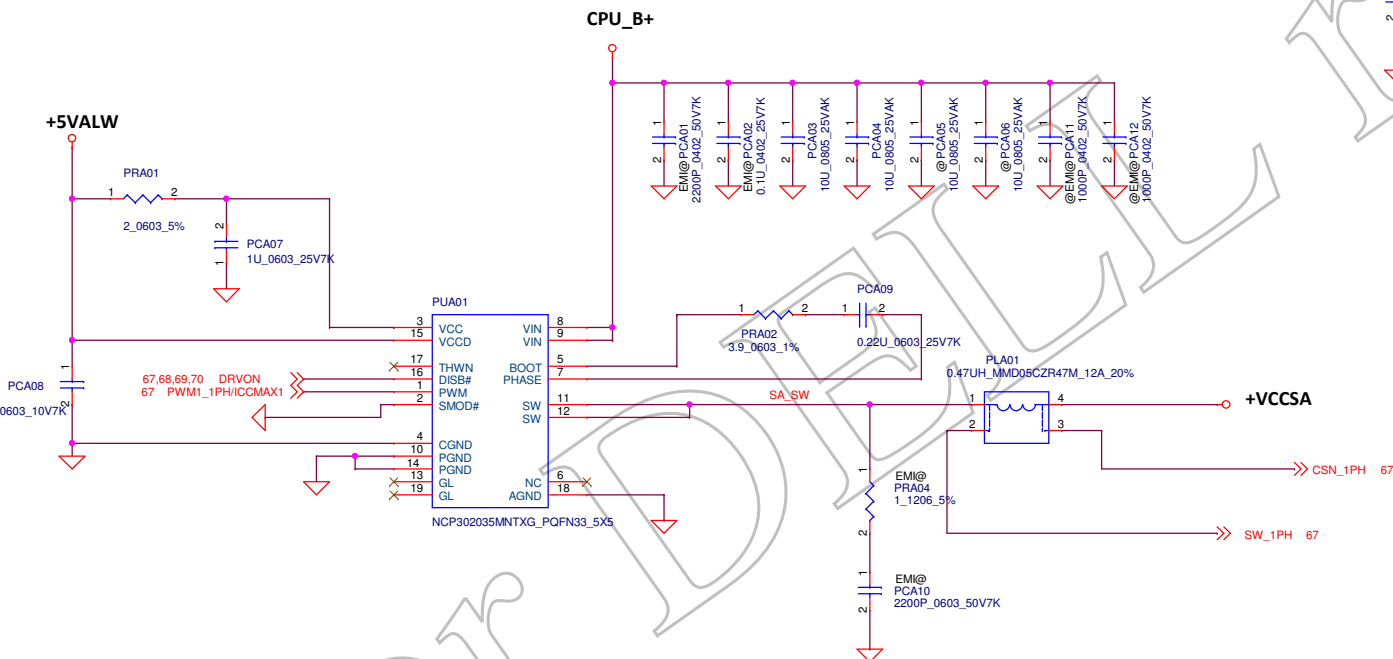
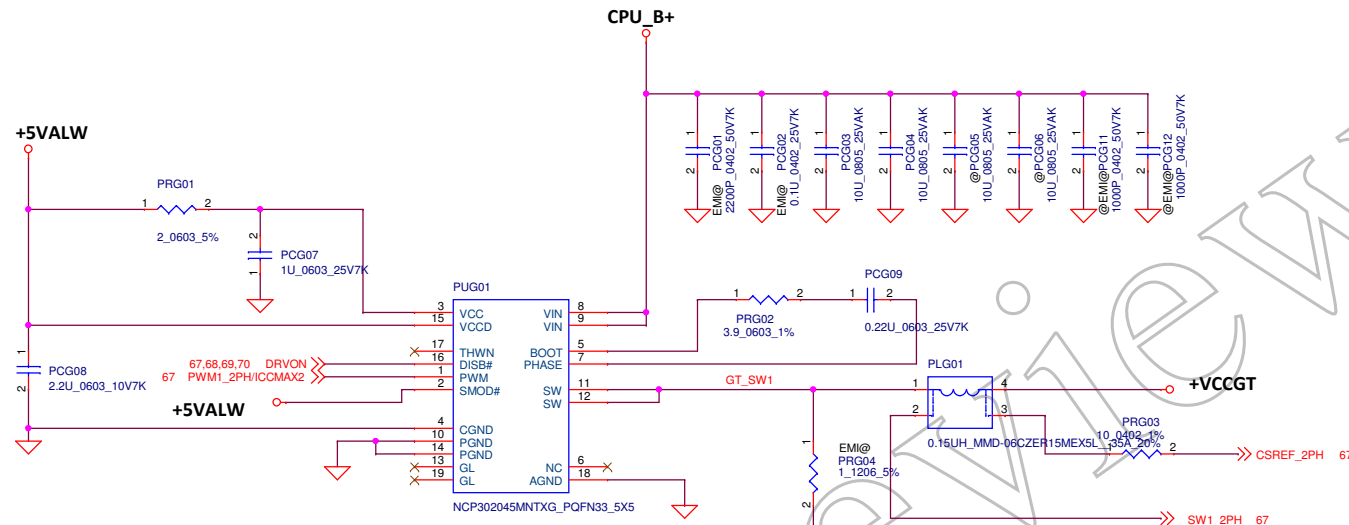
Main Func = CORE_Phase3&4



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Main Func = VCCGT/+VCCSA

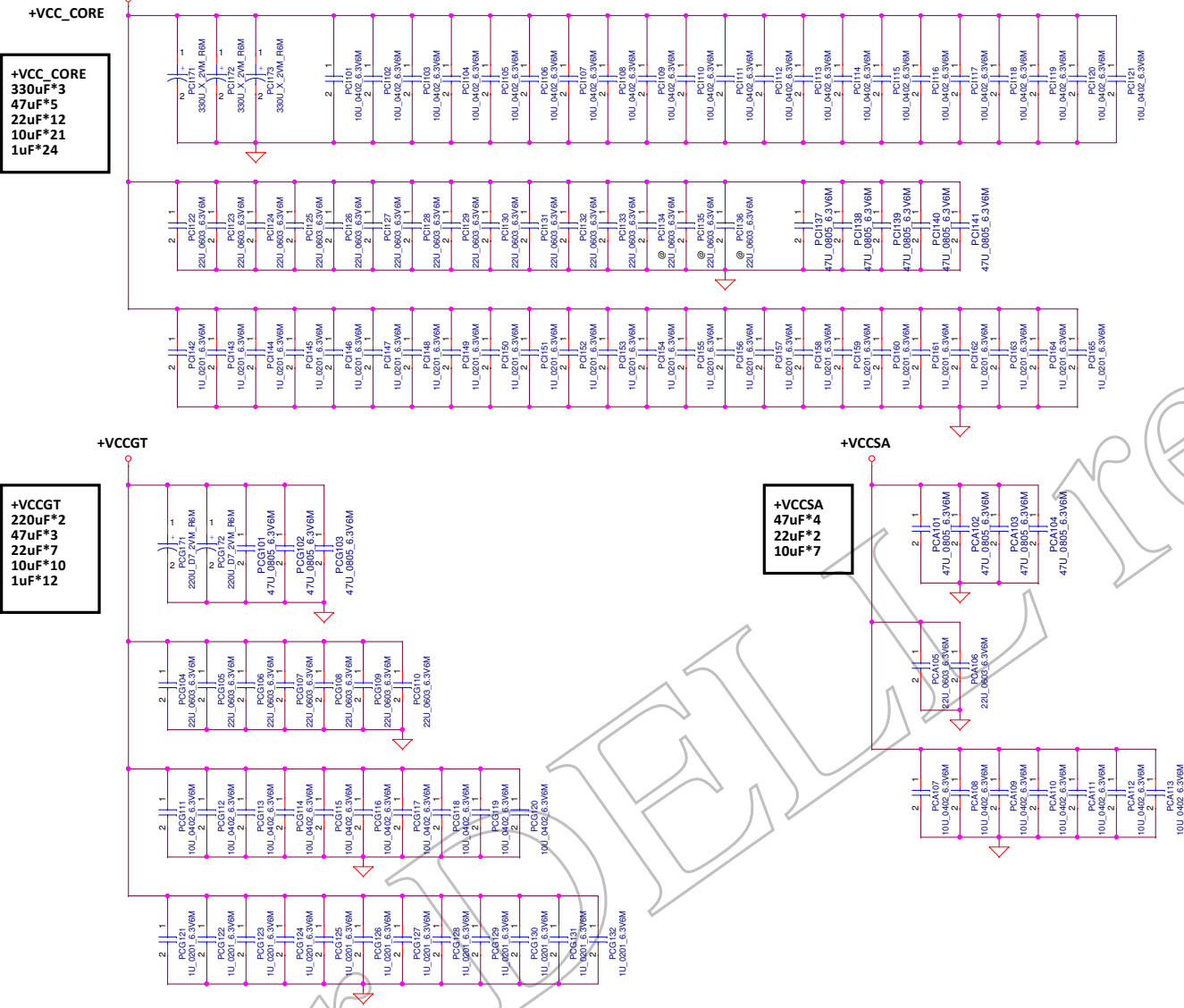
+VCCGT
TDC PL2 :25A
Peak Current 32A
OCP Current 39A
DCR 0.9mohm +/-5%
Load Line 2.7mV/A



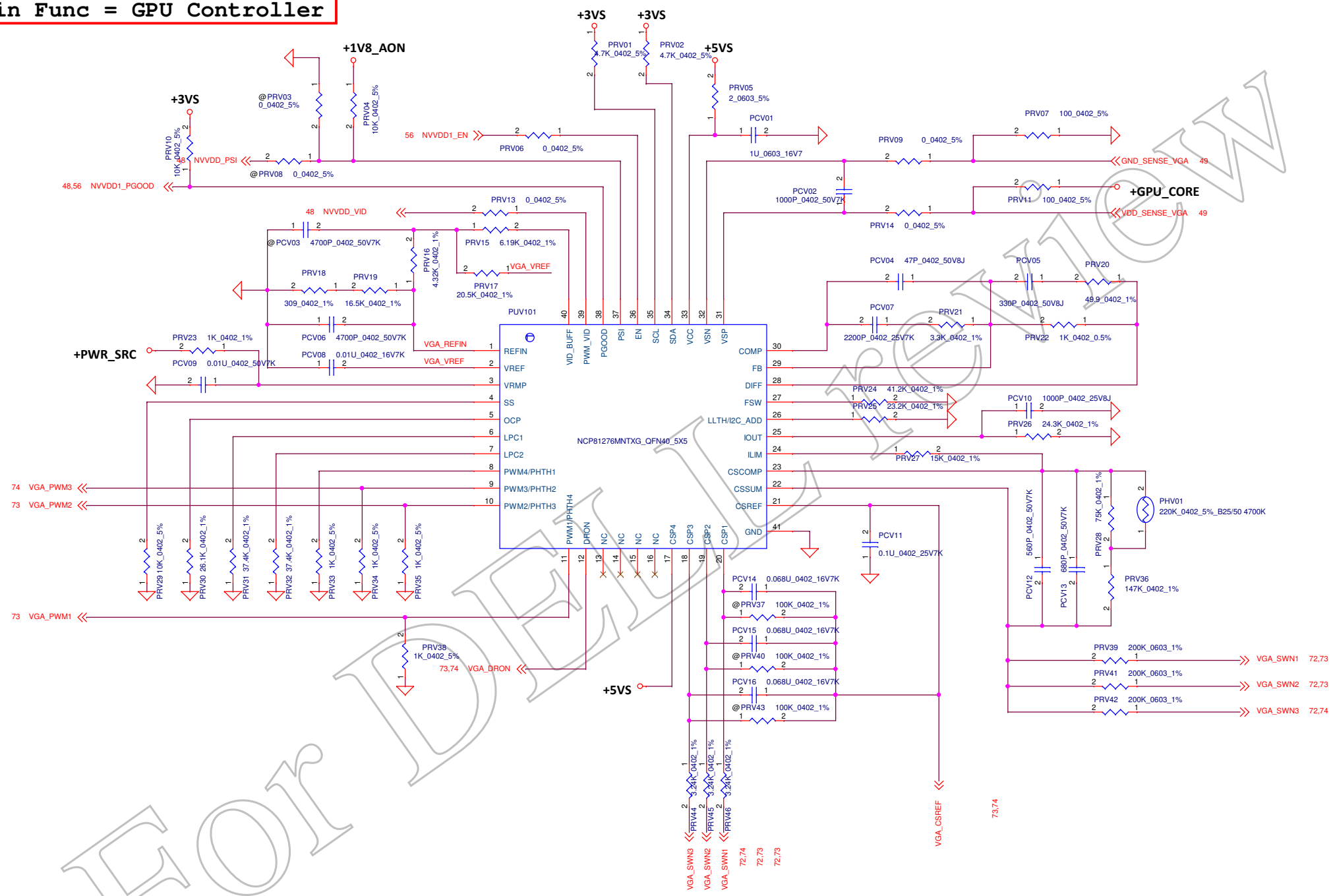
+VCCSA
TDC PL2 :10A
Peak Current 11A
OCP Current 13A
DCR 6.2mohm +/-5%
Load Line 10.3mV/A

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Main Func = PWR_CPU DECOUPLING



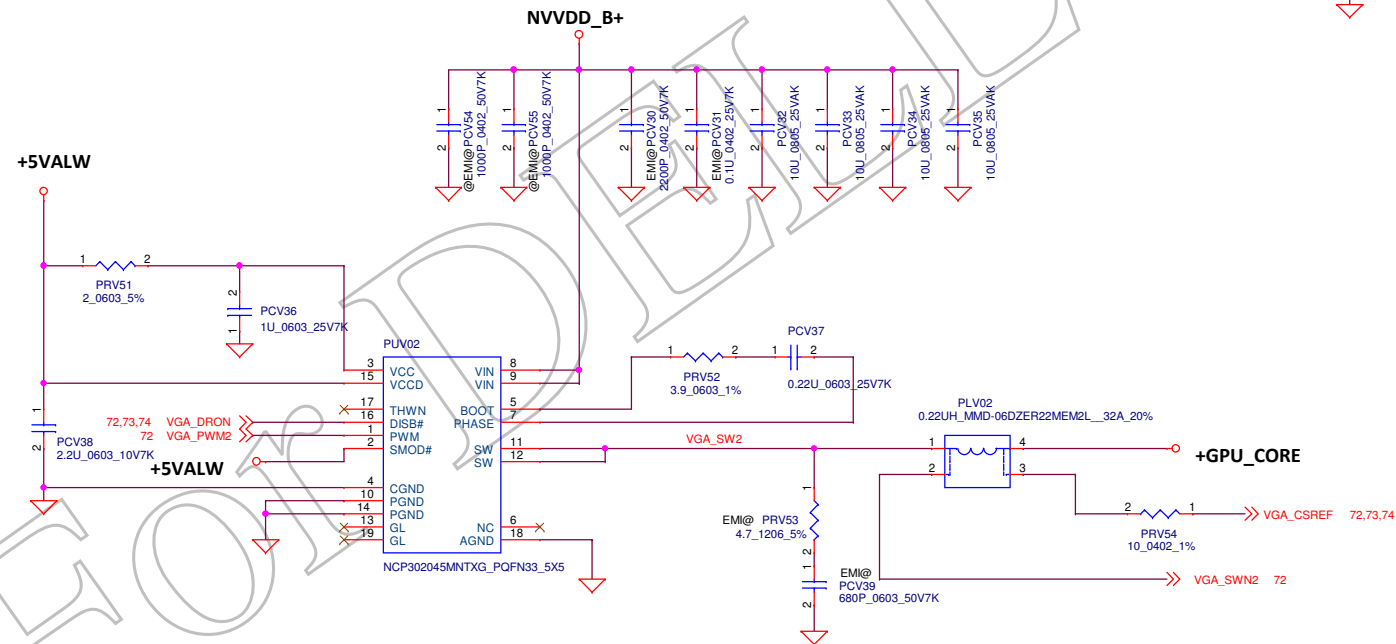
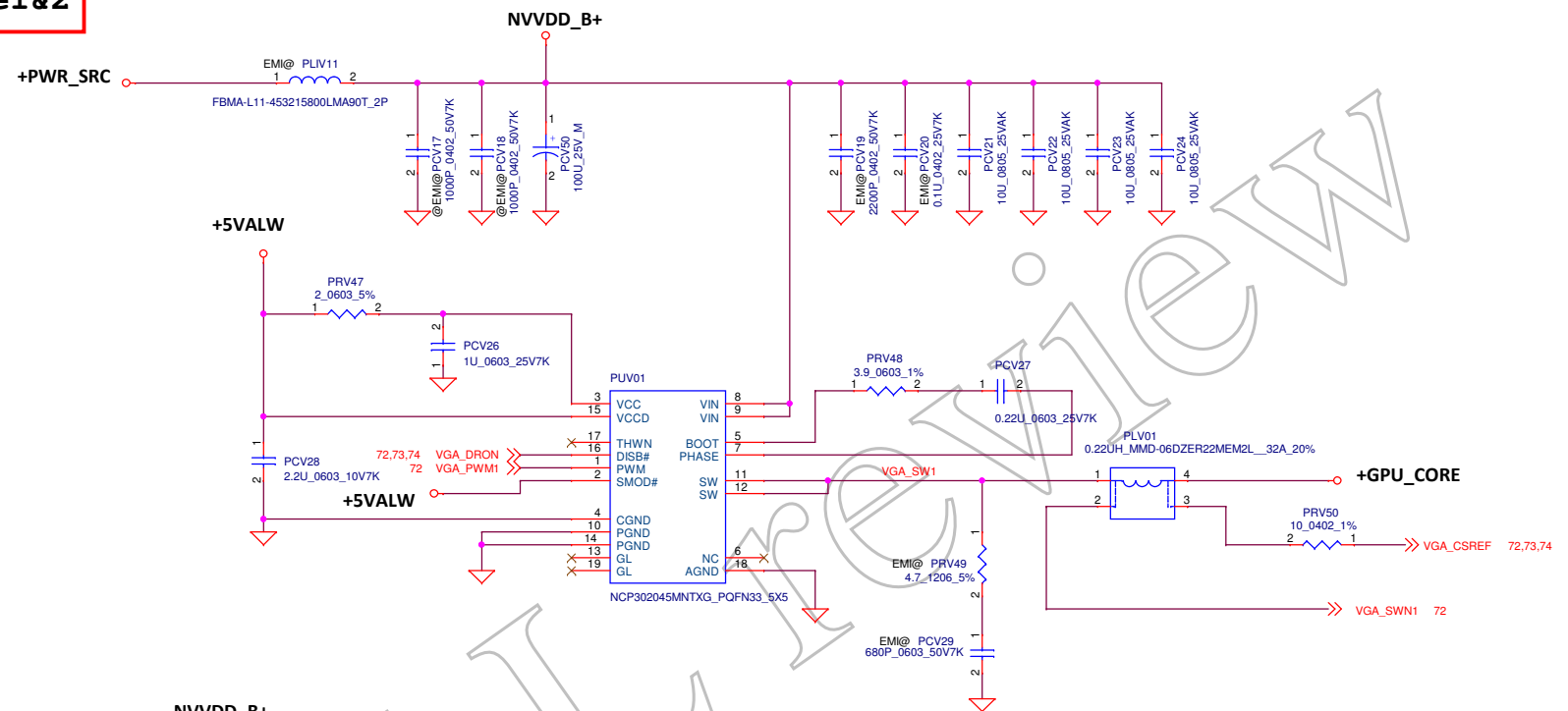
Main Func = GPU Controller



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Main Func = +GPU_CORE Phase1&2

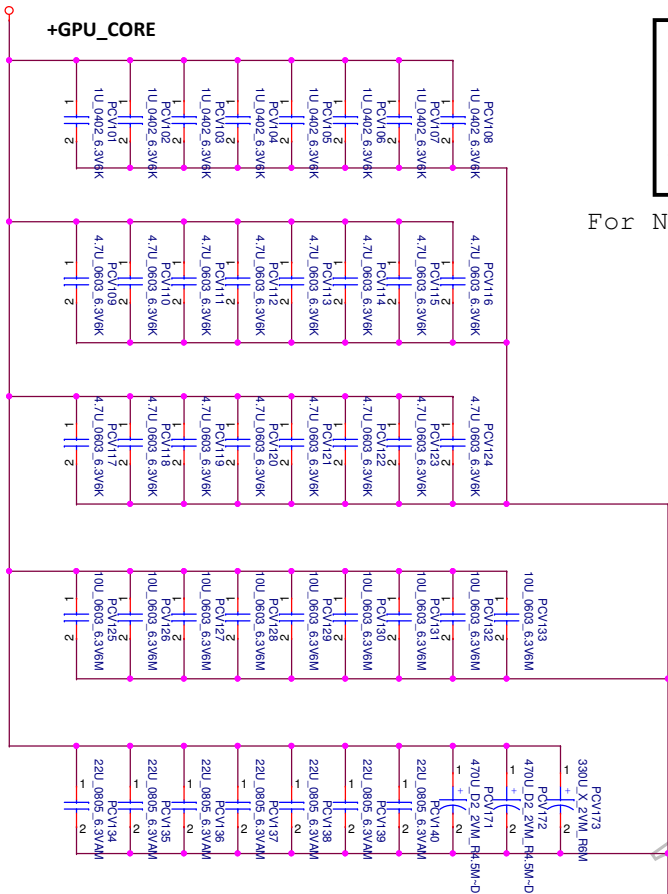
+GPU_CORE
TDC 59A (46+13)
Peak Current 124A (106+18)
OCP=149A
Fsw=305KHz
DCR:0.98mohm +-5%



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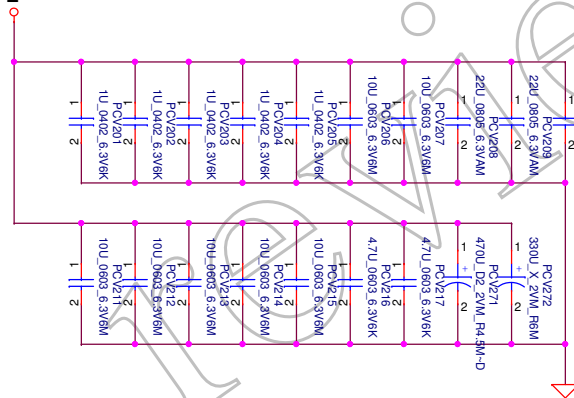
Main Func = VGA DECOUPLING



+GPU_CORE (NVVDD)
470uF X 2
330uF X 1
22uF_0805 X 7
10uF_0603 X 9
4.7uF_0603 X 16
1uF_0402 X 8

For NV N17P latest spec

+GPU_CORE

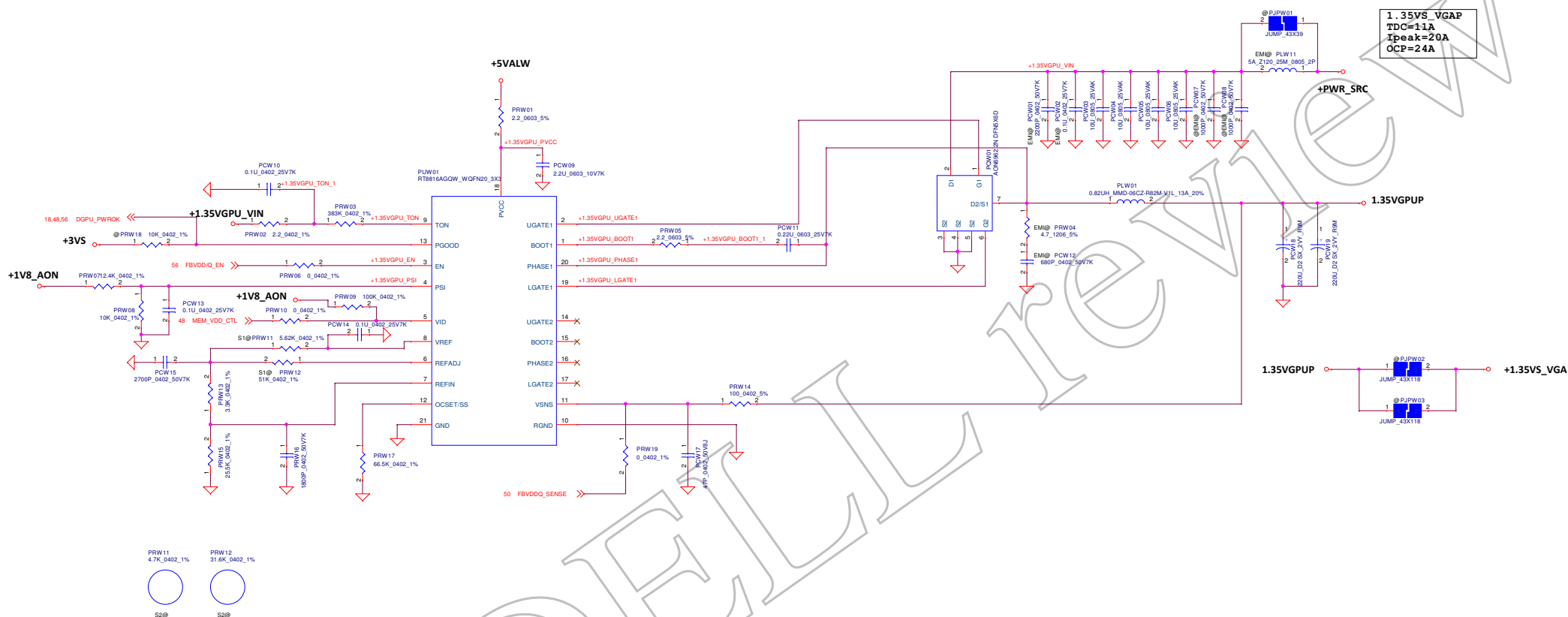


+GPU_CORE (NVVDD)
470uF X 1
330uF X 1
22uF_0805 X 3
10uF_0603 X 7
4.7uF_0603 X 2
1uF_0402 X 5

For NV N17P latest spec

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Main Func = +1.35VG PUP

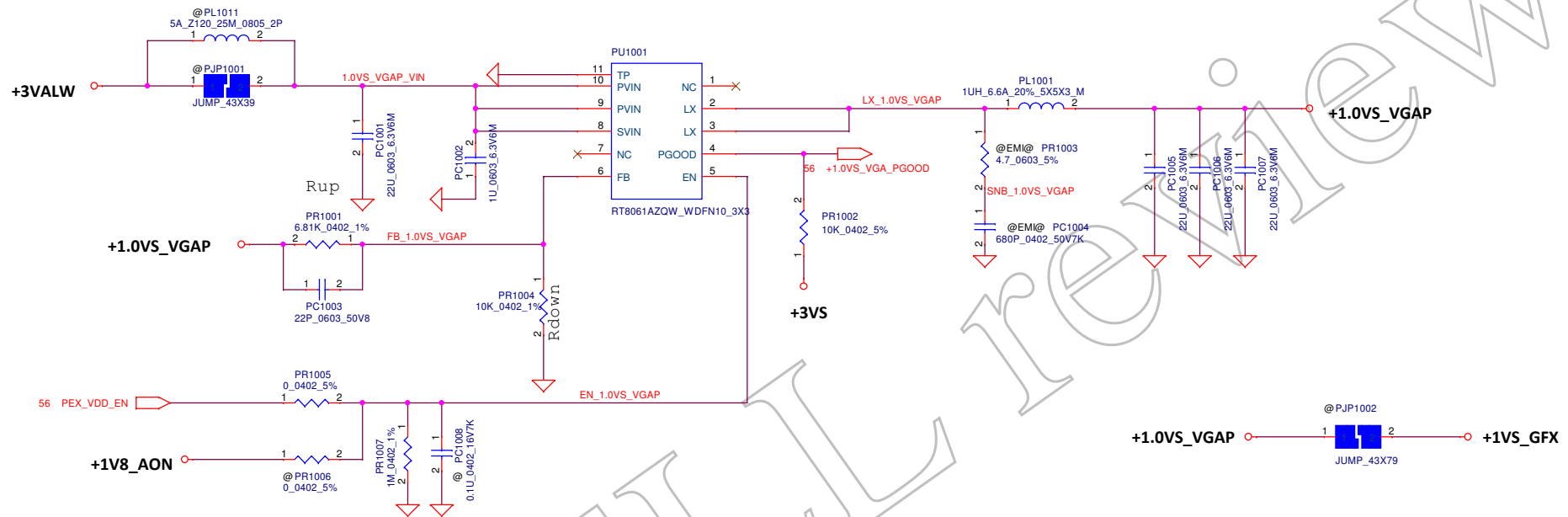


BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW11	PRW12
S1@ (4G)	N17P-G0/G1	256Mx32	Micron	1.35V & 1.5V	5.62K	51K
S1@ (4G)	N17P-G0/G1	256Mx32	Hynix	1.35V & 1.5V	5.62K	51K
S1@ (4G)	N17P-G0/G1	256Mx32	Samsung	1.35V & 1.5V	5.62K	51K
S2@ (3G/6G)	N17E-G1 Max-Q	128M/256M x32	Hynix	1.35V & 1.55V	4.7K	31.6K
S2@ (3G/6G)	N17E-G1 Max-Q	128M/256M x32	Samsung	1.35V & 1.55V	4.7K	31.6K

MEM_VDD_CTL	+MVDD
L	1.35V
H	1.5V/1.55V

Main Func = 1VS_GFX

+1VS_GFX
TDC 0.88A
Peak Current 1.1A
OCP current 4A



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